KU LEUVEN

ARENBERG DOCTORAL SCHOOL
FACULTY OF ENGINEERING SCIENCE

Alternative channel materials for 3-D NAND memories

Elena Capogreco

Dissertation presented in partial fulfilment of the requirements for the degree of Doctor of Engineering Science (PhD): Electrical Engineering

September 2017

Supervisor(s):
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In collaboration with

imec

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To my family

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Abstract

NAND flash memory has been the working horse of non-volatile storage in the last decades; its market has been experiencing an exceptional growth, which is supported by the increasing demand for portable devices. To satisfy the market demands, 3-D NAND flash memory technology, featuring poly-Si channel, has been introduced in mass production since 2014. However, the conduction in poly-Si channel is hampered by grain size and by scattering events at grain boundaries and charged defects. Furthermore, the current required for reading operations decreases as the number of stacked memory layers increases, making poly-Si unsustainable for long-term scaling.

This study focuses on the investigation of channel materials such as $In_xGa_{1-x}As$, with higher electron mobility than poly-Si, as a possible solution to enable further scaling for future 3-D NAND generations. The most challenging steps to integrate $In_xGa_{1-x}As$ by Metal Organic Vapor Phase Epitaxy are thoroughly discussed. A special attention is given to the surface preparation required to initiate the III-V growth. Two alternative surface preparation routes are investigated; their effect on the integrity and thickness of the memory stack, crucial for memory operation, is studied through physical and electrical characterization. A promising route is found and it represents an important step to achieve high mobility 3-D NAND devices. Furthermore, $In_xGa_{1-x}As$ channels with a diameter down to ~45 nm and different *In* concentrations, x, ranging between 0.25 and 0.55, are obtained by tuning growth conditions such as: temperature, choice of precursors and flow ratios. The conduction properties of $In_xGa_{1-x}As$ channels are then analyzed and benchmarked against the Si-reference, showing superior conduction properties for *In* concentration, x, higher than 0.45.

The results achieved in this research demonstrate that $In_xGa_{1-x}As$ is very promising as channel material for future generation 3-D NAND memories.

Samenvatting

NAND Flash geheugen is in de laatste decaden het werkpaard van niet-vluchtige opslag. De markt voor dit geheugen is uitzonderlijk gegroeid, gedreven door de stijgende vraag naar draagbare toestellen. Om aan deze marktvraag te voldoen is 3-D NAND Flash geheugentechnologie met polykristallijn siliciumkanaal (poly-Si) in massaproductie sinds 2014. De geleiding in dit poly-Si kanaal wordt echter beperkt door de korrelgrootte en door verstrooiing aan korrelgrenzen en geladen defecten. Bovendien daalt de stroom tijdens lees-operaties verder naarmate meer lagen gestapeld worden, waardoor poly-Si niet geschikt is voor lange termijn schaling.

Dit werk richt zich op het onderzoek naar kanaalmaterialen zoals $In_xGa_{1-x}As$ met hogere elektronenmobiliteit dan poly-Si, als mogelijke oplossing om verder schalen van 3-D NAND mogelijk te maken. De grootste uitdagingen voor het integreren van $In_xGa_{1-x}As$ door middel van Metallo-Organische DampFase Epitaxie worden uitgebreid besproken. Bijzondere aandacht gaat naar de oppervlaktevoorbereiding die nodig is om de III-V groei te starten. Twee alternatieve oppervlaktevoorbereidingsroutes zijn onderzocht. Hun effect op de integriteit en dikte van de geheugen-stapel die cruciaal is voor geheugenwerking zijn bestudeerd door fysische en elektrische karakterisatie. Een veelbelovende route is gevonden, die een belangrijke stap betekent naar het verkrijgen van 3-D NAND componenten met hoge mobiliteit. Bovendien zijn $In_xGa_{1-x}As$ kanalen met diameter tot 45 nm en verschillende In concentraties x verkregen door het afstemmen van de groeivoorwaarden zoals temperatuur, keuze van precursoren en stromingssnelheidsverhoudingen. De geleidingseigenschappen van deze $In_xGa_{1-x}As$ kanalen zijn geanalyseerd en vergleken met de silicium referentie. Deze vergelijking toont superieure geleidingseigenschappen voor In concentratie x hoger dan 0.45.

De resultaten van dit onderzoek tonen aan dat $In_xGa_{1-x}As$ veelbelovend is als kanaalmateriaal voor toekomstige generaties 3D NAND geheugens.

List of Acronyms

Acronym	Description
3-D	3-Dimension
A/R	Aspect Ratio
Al	Aluminum
ALD	Atomic Layer Deposition
Al_2O_3	Aluminum oxide
APM	Ammonia Peroxide Mixture
As	Arsenic
A-Si	Amorphous Silicon
BiCS	Bit-Cost Scalable
BL	Bitline
BlOx	Blocking SiO_2
BOTOX	Bottom SiO_2
BSG	Bottom Select Gate
BTBT	Band-to-Band-Tunneling
C	Carbon
C-AFM	Conductive Atomic Force Microscopy
CF_4	Carbon tetrafluoride
CG	Control Gate
Cl_2	Chlorine
CS	Crystallite Size
CT	Charge Trapping
CTLM	Circular Transmission Line Model
D	Drain
D_2	Deuterium
DF	Dark Field
DF-STEM	Dark Field Scanning TEM
DHF	Diluted Hydrogen Fluoride
EDS	Energy Dispersive X-Ray
Epi	Epitaxial
FA	Furnace Annealing

FG	Floating Gate
FGA	Forming Gas Atmosphere
FIB	Focused Ion Beam
FWHM	Full Width at Half Maximum
Ga	Gallium
GB	Grain Boundary
GI-XRD	Grazing Incidence X-Ray Diffraction
GS	Grain Size
GSL	Ground Select Line
H_2	Hydrogen
HAADF-STEM	High-Angle Annular Dark Field Scanning TEM
HCl	Chloridric acid
HDDs	Hard drive disks
hkl	Miller indexes notation
HR-TEM	High Resolution TEM
HTO	High temperature SiO_2
IGD	Inter-Gate Dielectric
IGS	Inter Gate Spacing
In	Indium
IPA	Isopropyl alcohol
IPD	Inter-Poly Dielectric
ISPE	Incremental Step Pulse Erasing
ISPP	Incremental Step Pulse Programming
LF	Light Field
LPCVD	Low Pressure Chemical Vapor Deposition
LTA	Laser Thermal Annealing
MBE	Molecular Beam Epitaxy
MLC	Multi-Level Cell
Mo	Molybdenum
MOS	Metal oxide Semiconductor
MOVPE	Metal Organic Vapor Phase Epitaxy
N_2	Nitrogen
NF_3	Nitrogen Trifluoride
NH_3	Ammonia
NH_4F	Ammonium fluoride
O_2	Oxygen
ONO	Silicon Oxide/Silicon Nitride/ Silicon Oxide
P/E	Program/Erase
Poly	Polycrystalline

PPD	Post Program Discharge
PVD	Physical Vapor Deposition
RBS	Rutherford Backscattering Spectrometry
RIE	Reactive Ion Etch
RTN	Random Telegraph Noise
RTP	Rapid Thermal Process
S	Source
SADP	Self-Aligned Double Patterning
SEM	Scanning Probe Microscopy
SG	Select Transistor
Si	Silicon
SiCoNi™	Trademark of Remote Plasma Assisted Dry Etch
SILC	Stress-Induced Leakage Current
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
SL	Sourceline
SLC	Single-Level Cell
SMArT	Stacked Memory Array Transistor
SONOS	$Si/SiO_2/Si_3N_4/SiO_2/Si$
SPM	Scanning Probe Microscopy
SSL	String Select Line
TAT	Trap Assisted Tunneling
TBAs	Tertiarybutylarsine
TCATs	Terabit Cell Array Transistors
TD-SEM	Top Down Scanning Electron Microscopy
TEGa	Triethylgallium
TEM	Transmission Electron Microscopy
TFT	Thin Film Transistor
TiN	Titanium Nitride
TLC	Three-Level Cell
TMGa	**T**rimethylgallium
TMIn	Trimethylindium
ToF-SIMS	Time-of-Flight Secondary Ion Mass Spectrometry
TOPOX	Top SiO_2
TSG	Top Select Gate
TuOx	Tunnel SiO_2
UV	Ultra Violet
W	Tungsten
WL	Wordline

List of symbol

Symbol	Unit	Description
I_D	A	Drain Current
I_{on}	A	On Current
I_{off}	A	Off Current
I_G	A	Gate Current
Rs	Ω/Sq	Sheet Resistance
μ	cm^2/Vs	Mobility
n_s	cm^{-2}	N-type sheet carrier density
p_s	cm^{-2}	P-type sheet carrier density
D_{Eq}	nm	Equivalent diameter
G_m	A/V	Transconductance
G_{mMAX}	A/V	Maximum transconductance
N_{grains}	---	Number of grains in the channel
$q\varphi_M$	eV	Metal Work Function
$q\chi_S$	eV	Electron Affinity
STS	mV/dec	Sub-threshold swing
R_{DS}	Ω	Drain to Source Resistance
[Ge]	at %	Ge content
[In]	at %	In content
[Si]	at %	Si content
GS	nm	Grain Size
τ	nm	Crystallite size
T_{Growth}	˚C	Growth Temperature
t_{Growth}	s	Growth Time
V_{th}	V	Threshold Voltage
ΔV_{th}	V	Threshold Voltage Shift
V_{Read}	V	Read Voltage
V_{pass}	V	Pass Voltage
V_G	V	Gate Voltage
V_{pgm}	V	Program Voltage
V_{WAIT}	V	Waiting Voltage

V_{sense}	V	Sensing Voltage
V_{DS}	V	Drain -to-Source Voltage
V_{SD}	V	Source-to-Drain Voltage
d_{hkl}	Å	Interplanar distance
a	Å	Lattice constant

List of publications:

1. **E. Capogreco**, A. Subirats, J. G. Lisoni, A. Arreghini, B. Kunert, W. Guo, C.-L. Tan, R. Delhougne, G. Van den bosch, K. De Meyer, A. Furnemont, J. Van Houdt, "Feasibility of $In_xGa_{1-x}As$ high mobility channel for 3-D NAND Memory," *IEEE Trans. on El. Dev.*, vol. 64, no. 1, Jan. 2017, pp. 130-136.
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5. **E. Capogreco**, J. G. Lisoni, C. Merckling, T. Numata, A. Arreghini, K. De Meyer, G. Van den Bosch, J. Van Houdt, "Electrical and physical characterization of Polycrystalline III-V compounds," *IEEE SISC*, 2014.
6. **E. Capogreco**, J.G. Lisoni, A. Hikavyy, A. Arreghini, E. Vecchio, T. Numata, C.-L. Tan, K. De Meyer, G. Van den Bosch, J. Van Houdt, "SiGe channel formation for 3D vertical channel transistor applications," *E-MRS Fall Meeting*, 2014.
7. A. Subirats, **E. Capogreco**, R. Degraeve, A. Arreghini, G. Van den bosch, D. Linten, J. Van Houdt, and A. Furnemont, "Channel and

near channel defects characterization in vertical $In_xGa_{1-x}As$ high mobility channels for future 3D NAND memory," in *Proc. IEEE IRPS*, 2016, pp. 6C.4.1-6C.4.5.
8. U. Celano, **E. Capogreco**, J.G. Lisoni, A. Arreghini, B. Kunert, W. Guo, G. Van den Bosch, J. Van Houdt, K. De Meyer, A. Furnemont, W. Vandervorst, "Direct three-dimensional observation of the conduction in poly-Si and $In_{1-x}Ga_xAs$ 3D NAND vertical channels," in *VLSI Symp. Tech. Dig.*, 2016, pp. 192-193.
9. G. Congedo, A. Arreghini, L. Liu, **E. Capogreco**, J. G. Lisoni, K. Huet, I. Toque-Tresonne, S. Van Aerde, M. Toledano-Luque, C.-L. Tan, G. Van den bosch and J. Van Houdt, "Analysis of performance/variability trade-off in Macaroni-type 3-D NAND Memory," in *Proc. IEEE IMW*, 2014, pp. 123-126.
10. J. G. Lisoni, A. Arreghini, G. Congedo, M. Toledano-Luque, I. Toqué-Tresonne, K. Huet, **E. Capogreco**, L. Liu, C.-L. Tan, R. Degraeve, G. Van den bosch, J. Van Houdt, "Laser Thermal Anneal of polysilicon channel to boost 3D memory performance, "in *VLSI Symp. Tech. Dig.*, 2014, pp. 24-25.
11. R. Degraeve, M. Toledano-Luque, A Arreghini, B. Tang, **E. Capogreco**, J. Lisoni, Ph. Roussel, B. Kaczer, G. Van den bosch, G. Groeseneken, J. Van Houdt, "Characterizing grain size and defect energy distribution in vertical SONOS poly-Si channels by means of a resistive network model," in *Proc. IEEE IEDM*, 2013, pp. 558-561.

Contents

Chapter 1

Introduction

Nowadays consumer's electronics such as smart phones, tablet, laptops, GPS navigators, health care devices, music players and digital photo/video cameras, are an inextricable part of the modern society and represent one of the fastest growing markets on earth; the steadily increasing demand for portable devices requiring data storage in huge volume, has triggered an exceptional growth of the non-volatile memory market. Non-volatile memories can retain the stored information even when not powered and there are various solutions available in the market to serve the need of different applications: hard drives, magnetic tapes, compact disks, NAND and NOR flash memories, etc.. Among them, the most popular for mass data storage application are hard drives and NAND flash. Hard drive disks (HDDs) use spinning magnetic platters paired with magnetic head to read and write data. On the other hand NAND flash is a semiconductor memory entirely implemented in solid state circuits and it does not require moving parts. Even if the cost per bit is relatively higher than HDDs, NAND flash has become a new driving force in the semiconductor industry over the last decade, thanks to its proven scalability [1], low power consumption and robustness, fundamental requirements for portable systems.

In order to overcome the scaling obstacle in conventional planar NAND Flash [2], 3-D NAND memory technology has been introduced for mass production for the first time in 2014 [3]. The scaling exploits the third dimension and consists in stacking vertically NAND cells on top of each other's; this approach leads to a significant bit-density increase with a reduced cost-per-bit. The most industrially relevant channel material for 3-D NAND is polycrystalline silicon (poly-Si). However, the conduction in

poly-Si channel is dominated by the presence of grains and hampered by scattering events at grain boundaries and charged defects [4]–[7]. As a consequence, the drive current required for reading operations is low, unstable and decreases as the number of stacked cells increases, rendering poly-Si unsustainable for long-term scaling.

This thesis is an effort to investigate alternative channel materials with higher electron mobility than poly-Si, as a possible solution to enable further scaling for future 3-D NAND generations.

1.1 Flash memories

A Flash memory is based on a Metal/Oxide/Semiconductor (MOS) transistor with a charge storage capability; compared to the conventional MOS device, the flash memory cell is characterized by an extra isolated layer serving to store the data, between the control gate (CG) and the substrate. Based on the nature of such layer, two types of memories can be distinguished: Floating Gate (FG), which was first introduced by Guterman *et al.* [8] and Charge Trapping (CT).

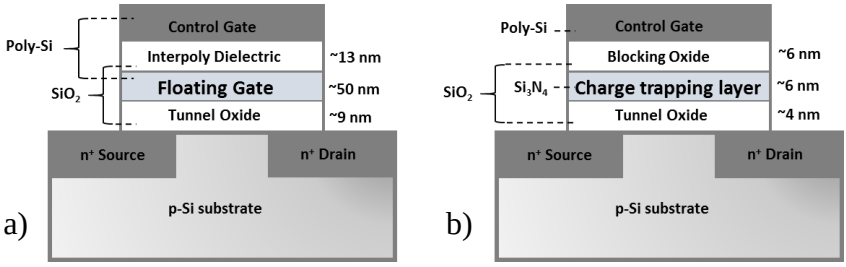


Figure 1.1: Schematic cross section of a) FG and b) CT memories. The thicknesses of the layers are taken from [9], [10].

The FG cell, shown schematically in Fig. 1.1.a, stores the data in a semiconductor layer made of poly-Si, while the CT cell, shown in Fig. 1.1.b, uses a dielectric made of silicon nitride (Si_3N_4). The first device using Si_3N_4 as a trapping material was proposed in 1967 [11]. The CT cell, built up as poly-Si/oxide/Si_3N_4/oxide/Si substrate, it is known as SONOS. Both FG and CT layers are sandwiched between two dielectrics: the bottom

oxide is made of silicon dioxide (SiO_2) and it is called Tunnel Oxide (TuOx), while the top one can differ: in the case of FG memory, the top oxide is a stack of $SiO_2/Si_3N_4/SiO_2$ (ONO) and it is called Interpoly Dielectric (IPD) or Inter-gate Dielectric (IGD), while in CT memory it consists of a SiO_2 layer called Blocking oxide (BlOx).

The digital information is stored in the FG/CT layers as an electric charge, which is able to modulate the threshold voltage (V_{th}) of the devices. The program operations consist of injecting electrons into the FG/CT through the TuOx and it results in a V_{th} shift of the devices in the positive direction, as shown in Fig. 1.2. On the other hand, the erase operation results in a V_{th} shift in the negative direction caused by the ejection of electrons from the FG/CT into the substrate.

In order to read the cell, a gate voltage called V_{Read}, is applied between the programmed and the erased V_{th} and the current flowing into the cell is measured: the level of current indicates whether the cell is in state '1' (erased state), or in state '0' (programmed state), as better described in the next section. This is the case of a single level cell (SLC), as shown in Fig. 1.3.a, where only two states are allowed and only 1 bit can be stored.

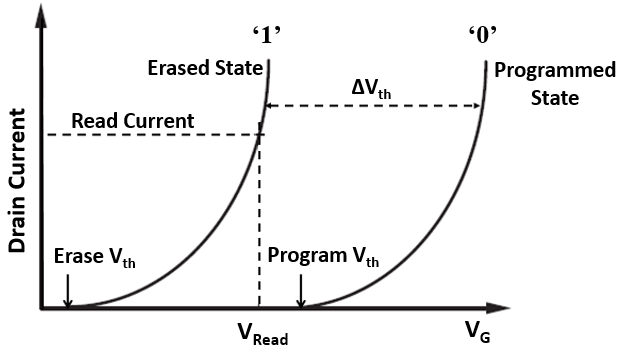


Figure 1.2: Drain current (I_D) versus gate voltage(V_G) of erased and programmed states.

When the V_{th} shift (ΔV_{th}) between erased and programmed state is large enough and the retention is good, it is possible to implement multi-level cells (MLC) [12]. For example a MLC can save up to 2bits/cell, which means that four different storage states can be distinguished: 00, 01, 10 and 11, as shown in Figure 1.3.b. In the same way, three-level cell (TLC) memories can save up to 3 bits/cell and have 8 different storage levels [13].

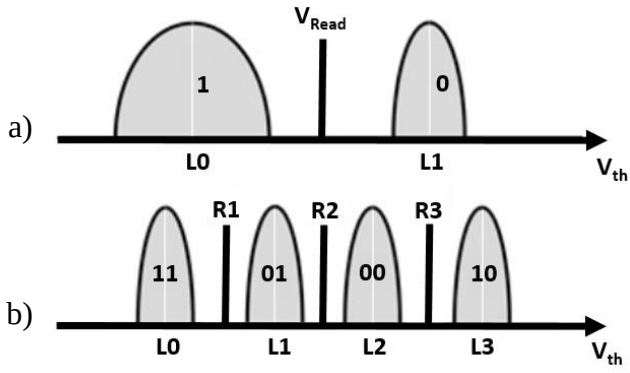


Figure 1.3: a) 1 bit SLC and b) 2 bits MLC [14].

In Fig. 1.3 the gap in between each voltage level represents the margin within which to apply the V_{Read}. As long as the storage levels do not cross the read points, data is accessed correctly. Moreover, the bigger the margin between these points, the more program/erase (*P/E*) cycles can be handled before failure. Each cycle weakens the TuOx, increasing the probability that electrons get trapped in the oxide itself. This phenomenon alters the transistor V_{th}, which in turn shifts bit placements, leading to cell failure [14], [15]. The cost per bit is cheaper for MLC as compared to SLC. However, the writing speed is slower and a higher read error rate requires a stronger error correcting code to be implemented [16], [17]. SLC memories are still preferred in applications where reliability and speed are more important than capacity.

1.1.1 Flash memories architectures

In order to achieve a high memory capacity per chip, memory devices must be organized in array structures. For Flash memories there are mainly two array architectures: NOR and NAND [18], as shown in Fig. 1.4.

In NOR scheme, depicted in Fig. 1.4.a, the cells are connected in parallel: the CGs of the cells in the same row are connected to the so called Wordline (WL). At the same time, the cells in the same column have their drain and source connected to the Bitline (BL) and Sourceline (SL), respectively. At the end of each BL there is a conventional transistor with the role to connect the output with the addressed column.

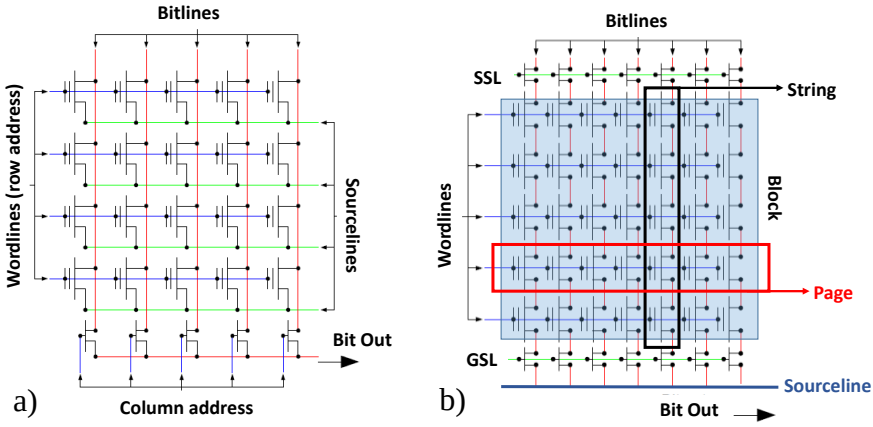


Figure 1.4: Schematic of a) NOR and b) NAND architectures.

The NAND architecture, shown in Fig. 1.4.b, is instead a true cross-point memory, as stripes of channels are crossed by stripes of gates (WLs): cells are connected in series forming a string. Each string can be selected by the select transistors, named string select line (SSL) and ground select line (GSL). Moreover, each string has only one contact to the BL and one contact to the SL. Figure 1.4.b also shows the "page" and the "block" parts: a page is defined as the minimum readable/programmable unit, while the block is the minimum erasable unit. As BL/GSL contacts are not required for each cell, NAND technology is the most dense circuit, allowing a minimum cell area of $4F^2$ (where F is the minimum feature size) against the $10F^2$ of the NOR array [19], [20].

NOR technology is more suitable for lower-density, high-speed read applications, known as code-storage applications [21]. On the other hand, NAND flash scheme allows faster program and erase, by programming pages and erasing blocks of data; it is ideal for low-cost, high-density, high-speed P/E applications, known as data-storage applications [21].

This thesis focuses on NAND Flash architecture, while more details on NOR scheme can be found in [18].

Figure 1.5 shows the typical voltages applied for read and P/E operations in NAND architecture.

During the **read operation** (Fig. 1.5.a), the page to be read is selected by setting the WL of interest to 0 V (V_{Read} = 0 V). All the other WLs are instead biased to a pass voltage (e.g., V_{pass} = 4.5 V). V_{pass} is chosen higher

than the maximum V_{th}, in order to create a conductive path and allow the BL to eventually discharge only as a function of the status of the selected cell. The selected BL is pre-charged to a fixed value [18]. If the selected cell is in erased state (V_{th} < 0 V), it sinks current and discharges the BL, so that the sensing circuitry will read "1". If the cell is programmed (V_{th} > 0 V), the conductive path is interrupted and as the BL cannot be discharged the sense circuitry will read "0". *P/E* operations in NAND flash are both performed by tunneling mechanisms [22]–[24].

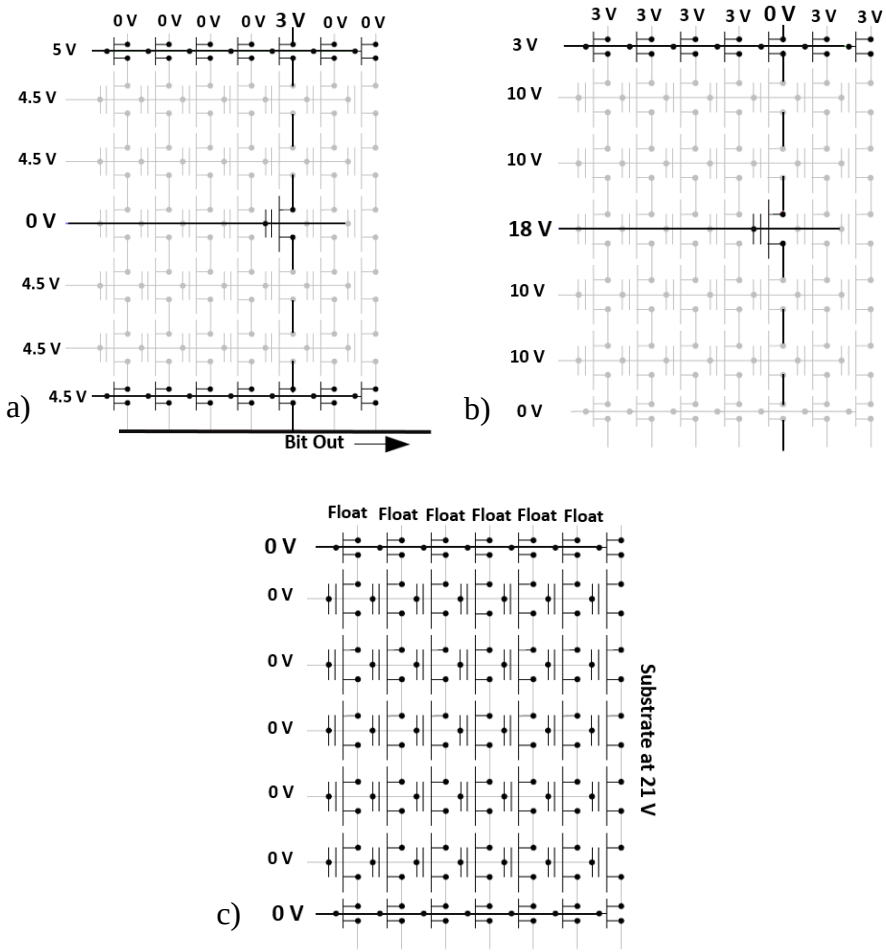


Figure 1.5: Typical voltages used to a) read, b) program and c) erase a cell in NAND architecture.

During the **programming operation** (Fig. 1.5.b), a high voltage (18-20 V) must be applied to the WL of the selected cell, to trigger a tunneling mechanism, as shown in Fig. 1.6. The gate of the SL is at 0 V, to block the I_D flow. The BL is biased at 0 V, to make sure that the total of the 18 V is applied to the gate stack, enabling charge injection. All the other WLs are biased to a voltage V_{pass} of ~ 10 V. V_{pass} has to be chosen high enough to guarantee the inversion of the channel and low enough to avoid programming of cells sharing the selected string. To avoid undesired disturbance by programming the cells sharing the same WLs of the selected cell, a bias of ~ 3 V is applied to all the unselected BLs; in this way the SSL is off and the channel voltage of the unselected strings increases, reducing the probability of electrons injection. There are also other techniques to boost the channel voltage, in order to avoid program disturbs and their details can be found in [15].

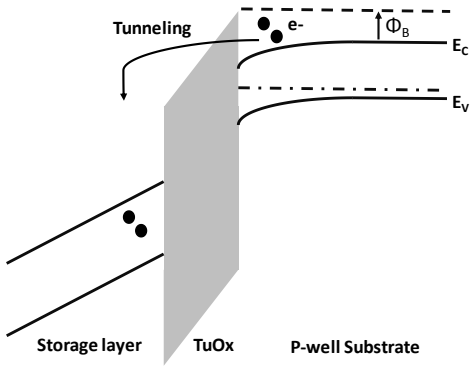


Figure 1.6: Band diagram of the tunneling mechanism in planar SONOS during programming [22].

In the NAND architecture the **erasing operation** is a "bulk operation"; this means that the erase bias is applied to the bulk terminal, which is shared between all the cells in a block. Therefore, unlike programming, which can be performed at page level, erase operation occurs for the whole block even if only a single bit has to be changed from "0" to "1" [18], by applying a high substrate voltage (~21 V) while keeping the BLs floating. In a CT memory two mechanisms contribute to the erase: the electrons detrapping from the CT layer and the holes injection from the substrate to the storage

layer [22]. In a FG memory the erase operation occurs only by ejecting the electrons from the storage layer

1.1.2 Memory operations

The characteristics typically used to assess the performance of a single flash memory cell are: *P/E* operation, Retention and Endurance. On the other hand, for cell arrays more aspects have to be taken into account such as read and program disturbs. These disturbs are not treated in this thesis and more details can be found in [24].

i. P/E operation: ISPE and ISPP algorithm

Independently of the charge injection/ejection mechanisms used for programming and erasing a memory cell, well-defined programming and erasing schemes are used to control the V_{th}. The standard procedures to program and erase a cell are referred to as Incremental Step Pulse Programming (ISPP) and Incremental Step Pulse Erasing (ISPE), respectively: *P/E* operations are divided in a number of *P/E* steps and at the end of each of them a *P/E* verify operation is applied.

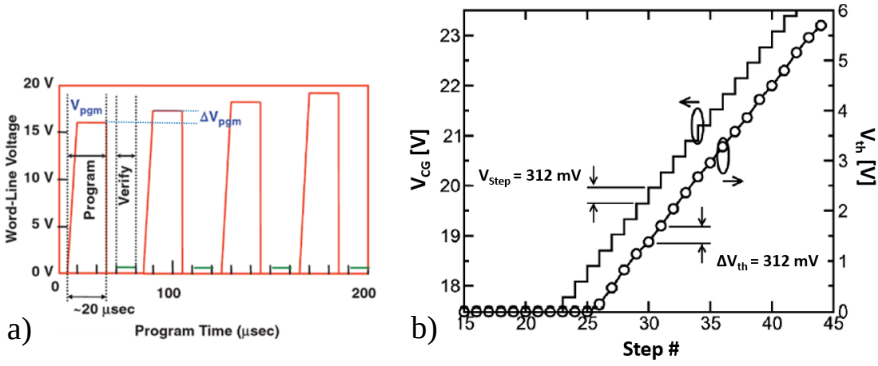


Figure 1.7: a) Example of an ISPP waveform [15]; b) example of an ISPP waveform used to program a 60 nm FG cell and the resulting V_{th} [25].

Figure 1.7.a shows an example of a program Voltage (V_{pgm}) "waveform" of an ISPP scheme [15]: initially a pulse with an amplitude of 15.5 V is

applied for 20 μs on the WL, then a program verify is performed to check whether or not the targeted V_{th} is reached.

The verify operation is almost the same as the typical read operation. If the targeted V_{th} is not reached, another pulse of increased amplitude is applied to the WL and the whole procedure is repeated until successful completion. In the example shown in Fig. 1.7.a the height of the subsequent pulses is incremented in steps of 0.5 V (ΔV_{pgm}**)** up to 20 V.

Figure 1.7.b shows that after an initial transient there is a linear relation between the ΔV_{th} and the V_{pgm} [25].

The ISPE algorithm (not shown) is similar to the ISPP one, but in this case a positive pulse is applied to the substrate rather than to the WL. The ISPP and ISPE procedures are able to compensate the cell-to-cell variations not only related to the process integration (e.g., spread in the TuOx thickness), but also related to the previous history of the cells, keeping a tight V_{th} distribution. These schemes become fundamental especially in MLC applications, where the placing of more than two levels for each cell requires an accurate control of the V_{th}. These algorithms present advantages also in terms of reliability; the TuOx degradation is mitigated, as only the minimum required charge flows through this layer.

ii. Retention

One of the key feature of flash memory is non-volatility, which is defined by the retention property. Retention is used to define the device's ability to hold the information (e.g., stored charge) and it is usually described by the P/E memory window, versus time. The memory window is defined as the difference between the programmed state and the erased state of the cell. Industrial specifications for silicon non-volatile memories usually indicate a retention of 10 years, which corresponds to $3x10^8$ sec and this specification should be met also at high temperature, typically 55/85 ˚C for consumer applications and 125 ˚C for automotive applications [26], [27].

iii. Endurance

Endurance property is one of the major reliability parameters for memory devices [28]. It is used to describe the ability of a device to withstand data rewrites, and hence to repeated *P/E* cycling stress. It is usually described by the program/erase memory window as a function of the number of *P/E* cyclings [29]. Writing operations forces electrical charges to flow through the TuOx, leading to the degradation of this layer [24]. After many *P/E* cycles, the dielectric can become so degraded that the

I_D–V_G characteristic is seriously altered. Industrial specifications indicate that each memory cell should support a minimum of 10^5-10^6 (depending on the application) *P/E* cycles [26]. *P/E* cycling can also greatly degrade the retention characteristics, as will be further discussed in the next section.

1.1.3 Limitations of planar flash memories

Both FG and CT flash cells share most of the scaling issues and limitations of the Metal Oxide Semiconductor (MOS) devices such as short channel effects, gate leakage, interface degradation [30]. However, compared to normal transistors, the situation is more critical for FG/CT memories, since cells must also preserve the stored information.

Scaling of FG cells down to 20 nm has been hindered by **Planarization** issues [31], [32]. In a conventional NAND FG cell, the CG and the IPD wrap around the FG, as shown in Fig. 1.8.a. The wrap-around serves to increase the capacitive coupling ratio between CG and the FG [25], [26], [33], so that most of the applied electric field will drop across the TuOx during the *P/E* operation; as a result, the amount of electrons injected in the FG is much higher than the one taken out through the IPD. For the 20 nm and below technology node, the cell spacing becomes too narrow to allow wrapping of the FGs with the CG. Therefore, the FG memories become planar, as shown in Fig. 1.8.b, leading to a reduction of the coupling ratio between CG and FG and to a consequent *P/E* saturation due to current flowing through the IPD [33], [34].

The continuous scaling has caused more **Parasitic Electrostatic Coupling** between adjacent FGs [35], [36], as shown in Fig. 1.9. The spurious cross-talk alters the device performance because data stored in the adjacent cells start to interfere with each other by capacitive coupling. This phenomenon becomes more serious when, due to the down-scaling of the cell only few electrons are stored in the FG; in such situation the logic state is more vulnerable to be disturbed by the interference, leading to an unstable state. In search for improving for this, the use of a high dielectric constant (high-k) material as IPD has been widely investigated in an attempt to overcome the geometrical limitation of planar FG memories [34], [37]-[39]. However, the high density of traps encountered in these high-k layers gives rise to reliability issues [40], [41] caused by the difficulties to remove the carriers from such defects.

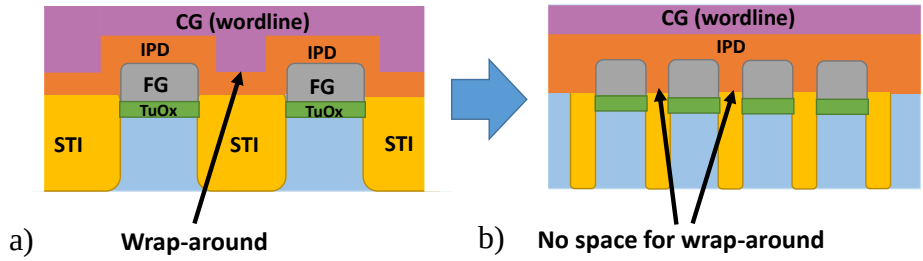


Figure 1.8: Schematic cross section of a) FG cells in wrap-around configuration and b) FG cells without sidewalls (wrap-around).

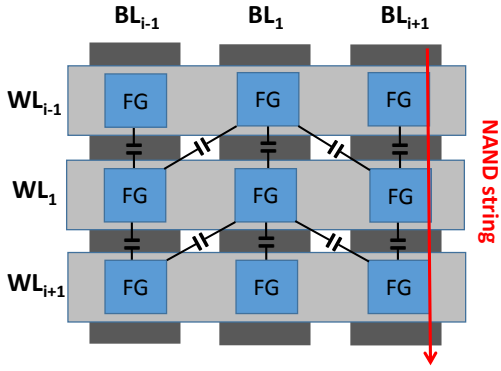


Figure 1.9: Parasitic capacitance between adjacent cells in FG memory arrays.

Flash memory compatibility with CMOS forces to scale the operational voltages [30], [42]. This means that the TuOx thickness must also scale. However a thinner TuOx offers a less effective barrier for the electrons inside the FG/CT, compromising the retention characteristics. In addition, the device capacity to store charges also degenerates over time. The degradation of the TuOx after repeated *P/E* stress can cause stress-induced leakage current (SILC), as shown in Fig. 1.10.a, associated with generated traps. Each trap represents an allowed energetic state inside the oxide bandgap and it becomes an intermediate step used by a carrier to escape out of the FG through trap-assisted tunneling (TAT) [41]–[43].

The CT memory approach appears more favorable than the FG one. The advantage of using CT memories instead of FGs is reflected by their

stronger scaling ability [42], planarization and significantly reduced capacitive coupling ratio between adjacent cells, as the carriers are stored further from the electrode boundary. Indeed, in a FG device the electric charge accumulates at the interfaces with the insulating barrier and can freely flow. Contrary to the FG, in the CT memory the carriers are trapped on localized traps levels distributed throughout the whole of the dielectric layer and cannot freely move; this means that a defect in the TuOx would only cause a partial loss of the carriers locally stored near the degraded TuOx, reducing the impact of the SILC, as shown in Fig. 1.10.b. In CT memories the BlOx is made thicker than the TuOx to guarantee preferential tunneling from the substrate to the trapping layer and to avoid leakage from Si_3N_4 to the CG. However, planar SONOS still exhibits retention problems, as charge carriers can leak from the nitride layer through the thin TuOx by tunneling [42].

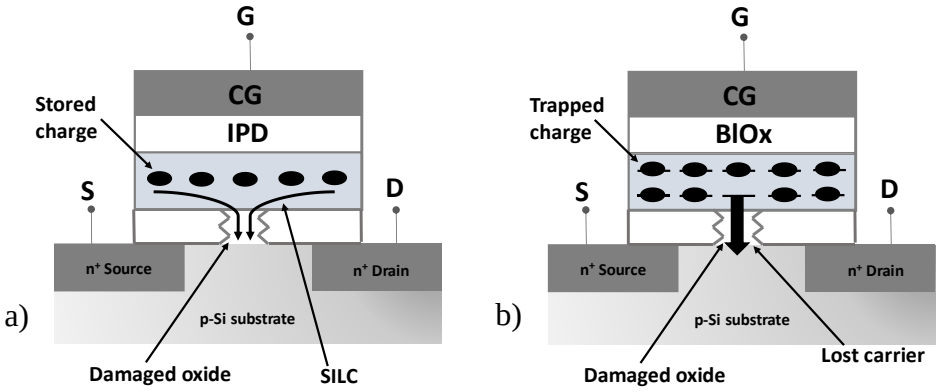


Figure 1.10: SILC current in a) a FG device and b) a CT device.

Lots of efforts have been made to improve the characteristics of CT flash memory including the engineering of the CG, BlOx and TuOx [44], [45]. Despite all the efforts made to shrink the dimension of both FG and CG, the ultimate scaling limit for planar Flash memories is imposed by lithographic limitations as the dimensions of the cells become smaller. To manufacture a 20 nm NAND cell, advanced cell pitch reduction techniques such as Spacer Assisted Double Patterning or Self-Aligned Double Patterning (SADP), are used for critical lithographic steps [46]. In brief, SADP allows to produce features at geometries half as wide as the printable

resolution on the wafer. But SADP has its limit too and to pattern below the 20 nm design rule, quad patterning technology has to be used. Double patterning makes difficult to control exact features and tolerances. Therefore, it is not difficult to imagine how quadruple patterning amplifies this challenge. In addition, such technique is extremely difficult and too expensive to be introduced in Flash memory production [46].

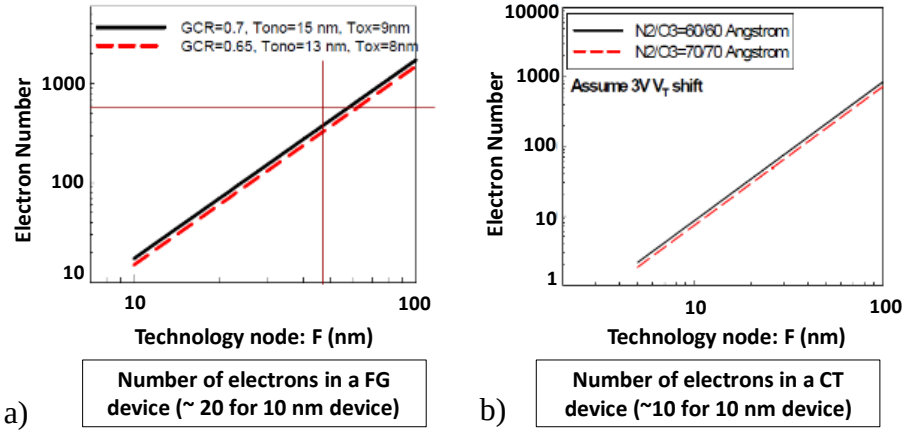


Figure 1.11: Estimation of the number of electrons that can be stored in a a) FG, b) CT memory cell as the technology node is reduced [32].

By shrinking the dimension of both FG and CT, the number of electrons that can be stored decreases [32], [34]. Figure 1.11 shows that the number of electrons in the storage node decreases with the area of both FG and CT NAND memory. For example, for a technology node of 10 nm, 20 electrons can be stored in a FG cell and only 10 electrons in a SONOS [32]. The number of captured charges involved in distinguishing between logic states becomes so small that memory performance and reliability starts to represent a big concern. As the pitch decreases, the ΔV_{th} introduced by a single electron increases drastically [47]. The deviation introduced by a single electron causes uncorrectable overlaps between the different states of MLCs, leading to unreliable device operation.

The scaling down of planar Flash memories cannot be continued indefinitely; that's why the approach to add a new dimension to the memory array, e.g., 3-Dimension (3-D) memories, has been proposed in the last decade, as discussed in the next section.

1.2 From planar to 3-D NAND memories

In order to overcome the scaling limitations imposed by planar memories, vertical 3-D NAND memory technology is nowadays in production. 3-D flash memory is based on the concept to increase the bit density without shrinking down cell size, but just building up in height. In 2014, Samsung was the first company to commercialize Vertical 3-D NAND memory based on CT technology [3]. Currently all the other major 3-D NAND players on the market, such as Micron, SK-Hynix, Toshiba-SanDisk, have their own and unique cell structure in 3-D, with differences regarding FG-based and CT-based cells as well as different number of stacked layers: SK-Hynix is producing a TLC 3-D NAND with 48 layers and the company has already announced that is planning to introduce 72 layers by the end of 2017 [48]. Toshiba-SanDisk and Samsung have already started the production of TLC 3-D NAND with 64 layers [49]-[51], while Micron produces a 32 layers TLC 3-D NAND. Remarkably, Micron is the only company to still use a 3-D NAND product based on FG technology [52], [53].

The idea to integrate NAND flash vertically was first proposed by Toshiba in 2007 with the Bit-Cost Scalable (BiCS) memory array [54]. The technology name comes from the fact that the bit cost scales down with increasing number of layers while the number of critical lithography steps remains constant [54].

So far several approaches have been proposed to vertically stack NAND cells [54]–[61]: most architectures are based on CT memories, although Hynix has proposed a 3-D NAND flash array based on FG [61] and Micron is producing it. However, among all of the suggested 3-D NAND architectures, BiCS, terabit cell array transistors (TCATs) and Stacked Memory Array Transistor (SMArT) [54], [55], [60], are considered the most promising and all of them share the same principle: the traditional planar transistor is turned 90 degrees and presents a cylindrical poly-Si channel with multiple gates all around, as shown in Fig. 1.12.b and Fig. 1.14.

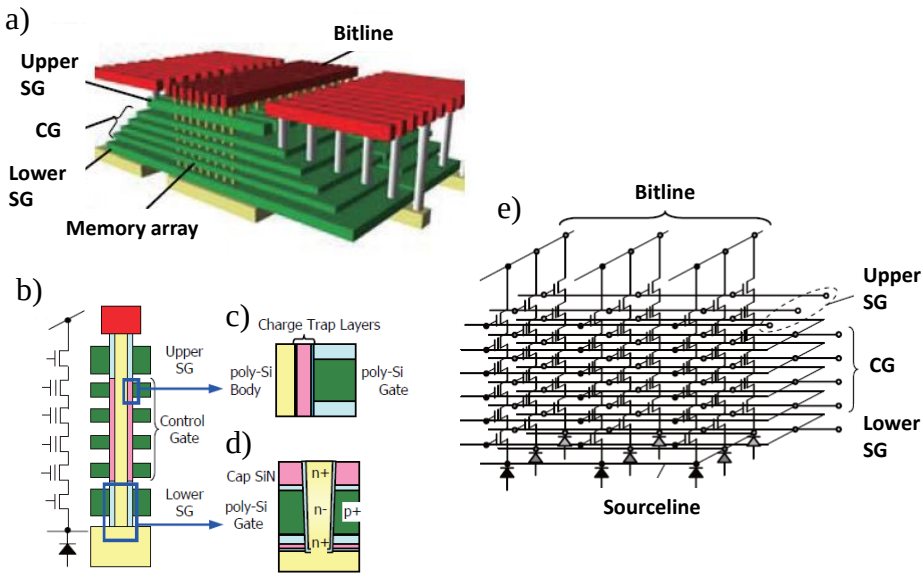


Figure 1.12: a) Schematic of BiCS technology. Cross sections views of b) the string, c) the cell, d) the lower selector. e) Equivalent circuit of BiCS [54].

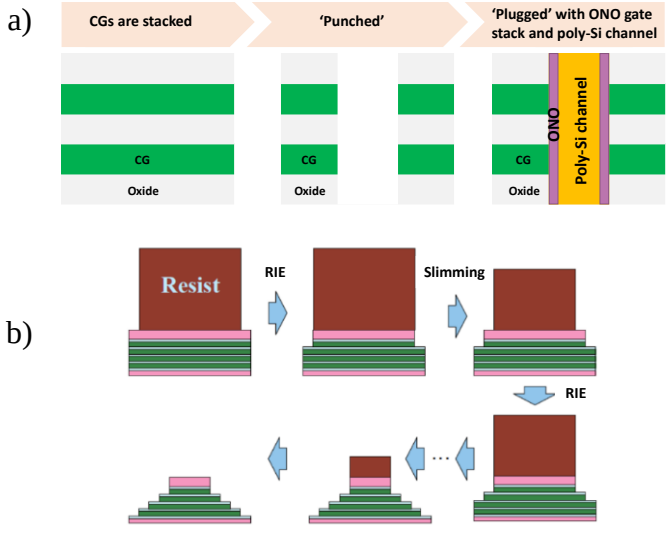


Figure 1.13: a) Main fabrication steps of BiCS array and b) subsequent reactive ion etch (RIE) steps required to obtain a staircase structure [54].

The BiCS-like architecture, shown in Fig. 1.12.a, is fabricated by a gate-first channel-last approach. The poly-Si CGs, depicted as the green word planes in Fig. 1.12.b, are stacked vertically on top of the yellow Sourceplane and of the lower select transistors (SG), reported in Fig. 1.12.d. Both the Sourceplane and the lower SG are created in separate steps [54].

Figure 1.13 shows in detail the main fabrication steps of BiCS: the formation of the word planes stack consists of the deposition of poly-Si CGs interleaved by oxide. Next, a punch-and-plug approach is used: vertical cylindrical memory holes are first punched through the entire word planes stack and then plugged with ONO gate stack and the poly-Si channel, as sketched in Fig. 1.13.a. To contact each CG, the word planes stack must be etched into a staircase structure by slimming down the photomask with subsequent Reactive-Ion-Etching (RIE) steps [54], as shown in Fig. 1.13.b. In order to minimize disturbs, each block of memory holes is separated from each other by creating a slit [55]. Then, the upper SG are formed and cut into lines, which will work as row address selector. Finally the channels are connected to the red bit lines, as shown in the sketch of Fig. 1.12.a and Fig. 1.12.b. The resulting BiCS circuit is shown in Fig. 1.12.e.

Contrary to the BiCS technology, where the CGs are deposited before the channel deposition, TCAT and SMArT technologies, as illustrated in Fig. 1.14, follow a gate-last approach, which is required to replace the poly-Si word planes with metal. The typically used CG material is tungsten (*W*). The advantages of the metal gate replacement are: better *P/E* and the reduction of the resistivity of the WL [55].

In the TCAT technology an oxide/nitride stack is deposited instead of oxide/poly-Si. The channel is always formed through a process of punch and plug. But unlike the BiCS technology, which uses a poly-Si full channel, TCAT and SMArT schemes use poly-Si Macaroni channel, as shown in Fig. 1.14.c and Fig. 1.14.d. The concept of Macaroni was presented for the first time in 2007 by Toshiba [62]. A Macaroni channel consists in a very thin poly-Si layer deposited at the sidewalls of the cylindrical memory hole. The central hole is instead filled with oxide. The advantage to use a thin poly-Si liner is that the channel can be better controlled by the CG [62].

To allow the metal-gate replacement, a WL cut is made through the whole stack between each row of poly-Si channel, as shown in Fig. 1.14.b. The sacrificial layer of nitride is then etched and replaced with the ONO gate stack and the metal CG. The reason why the metal is not directly deposited during the formation of the word planes is because it cannot withstand the

thermal budget involved with the materials deposited after (such as the poly-Si channel, etc.) and the mechanical stress.

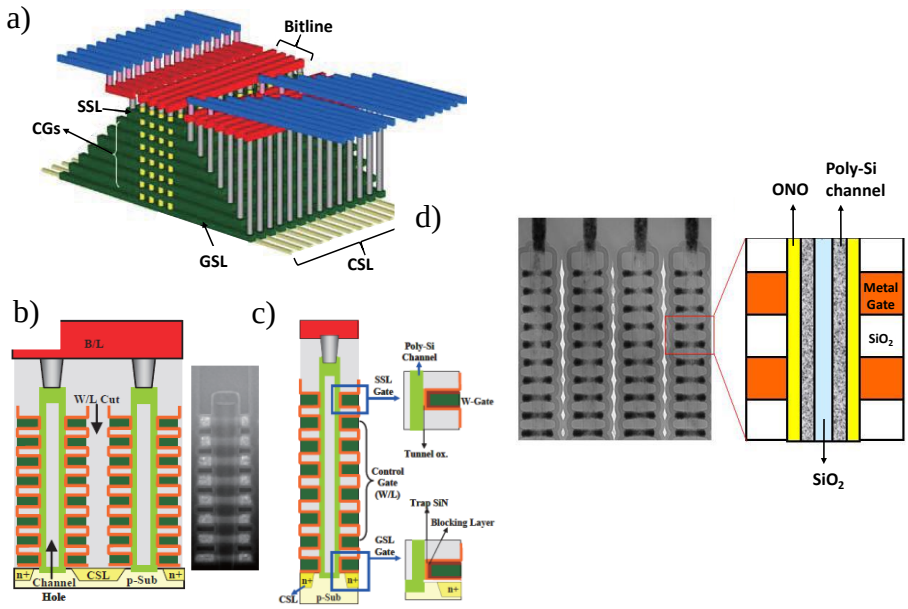


Figure 1.14: a) Schematic of the TACT technology; Cross section views of b) the WL cut in TCAT, c) the string of TCAT, d) the string of SMArT [55], [60].

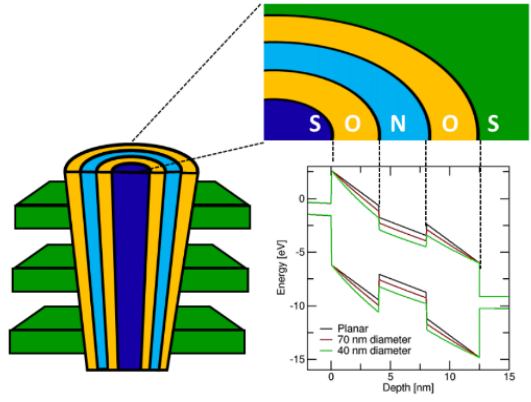


Figure 1.15: Cross-section of a 3-D SONOS channel showing the band-diagram during programming for different channel diameter [65].

The SMArT technology is similar to TCAT, with the exception that in SMArT scheme the stack height is minimized by inserting ONO layer directly in the plug, as shown in Fig. 1.14.d. Indeed, contrary to TCAT, where the ONO is deposited after the WL cut, which reduces the possibility to scale further the CG, in the SMArT scheme the ONO is deposited just prior to the channel formation and runs vertically.

The main advantage of vertical 3-D NAND is that the critical dimensions (CD) requirements are relaxed [63], [64]. Moreover the typical memory performance problems faced by planar SONOS are circumvented thanks to the cylindrical geometry [65], [66]. The electric field in the channel is concentrated where the curvature is high (or the diameter is small), causing a band-bending, as shown in Fig. 1.15. Therefore preferential tunneling will occur in the TuOx rather than in the BlOx, enhancing the *P/E* window [66]. Reading and *P/E* operations in 3-D NAND are essentially the same as in planar NAND. Of course, the sizes of the pages and blocks differ based on the number of stacked layers.

The mechanism involved to *P/E* a 3-D NAND cell is still tunneling, with some exceptions for the erasure of BiCS. [54].

1.2.1 Limitations of 3-D NAND memories

a) Film stack deposition

The 3-D NAND manufacturing process starts with depositing multiple alternating layers of materials such as thin layers of oxide/nitride or oxide/poly-Si. The film thickness determines the gate length. Any defect or small variation in film thickness can result in a large deviation at the top of the stack, as shown in Fig. 1.16.a, leading to a poor device performance. Therefore, highly uniform and smooth deposition, layer-to-layer precision and adhesion are required. In addition, film stress management becomes critical and more challenging with increasing the number of stacked layers, which in turn is required to achieve cost-effective production.

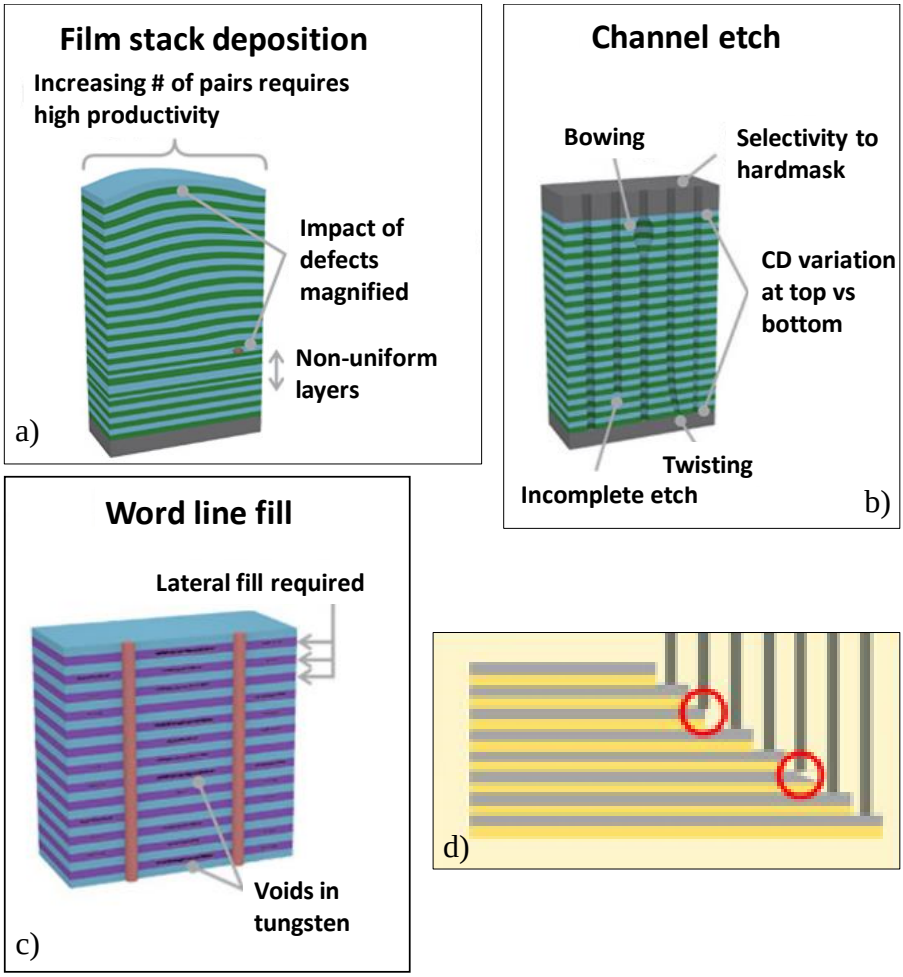


Figure 1.16: Main challenges for 3-D NAND fabrication during a) film stack deposition, b) channel etch, c) WL etch and d) staircase formation; un-landed contacts are highlighted with circles [67], [72].

b) Channel hole etching

The channel hole etch represents one of the most challenging processes due to both the high aspect ratio (A/R) and the different materials involved in the word planes stack. The A/R for 3-D NAND holes is more than 40:1, against the 10:1 for planar NAND [67], [68].

Due to the high A/R, tall and narrow features tend to distort, causing channel bowing and twisting(Fig. 1.16.b), that could lead to shorts or

interference between neighboring memory strings. Even if these effects can be avoided by using a highly selective etching process, the memory hole will never achieve a perfect cylindrical hole, but rather a cone shaped hole. This phenomenon will get worse with longer channels [69] and devices positioned near the bottom of the string will have a smaller diameter than the ones in the top part. Since the electrical field is more concentrated in smaller diameters, devices close to the bottom will show faster *P/E*, but also worse retention as trapped electrons can tunnel back easier [70]. Devices with different performance within the same string compromise the operation of the whole memory array.

c) Filling between small gaps

In the case of replacement-gate architectures, additional critical steps such as the filling of metal word planes via the WL slit is required. The metal deposition, which is done by the Atomic-Layer-Deposition (ALD) process [71], has to be extremely accurate to avoid possible voids in the metal gates, as shown in Fig. 1.16.c. Moreover, electrostatic force may cause collapse of features when sacrificial layers of nitride/poly-Si are removed to be replaced by metal.

d) Patterning and contacts formation

Another bottleneck in the memory array formation is represented by the staircase etch of the word planes stack and the formation of contacts and bit lines (BL). Stair-step etch is a completely new process developed ad-hoc for 3-D NAND [72]. The etching is a tricky step because it must be precisely controlled to make each via aligned with its poly-Si/metal word plane. Moreover, the thinner the gates, the more difficult the staircase formation becomes. As a consequence, the etching could not result in a straight profile. The tapered edge on a step can in turn cause un-landed contacts, as highlighted with red circle in Fig. 1.16.d, leading to the failure of the entire block.

e) Poly-Si channel in place of single crystal

Contrary to the single crystal Si channel of planar NAND technology, the industry uses poly-Si as channel material for 3-D NAND. If on the one hand poly-Si is a solution more economical, on the other hand it brings additional problems.

As every polycrystalline material, poly-Si consists of single crystals, called grains, with different crystallographic orientations [73], [74]. The

dimension of each grain can be in the order of micrometers or nanometers, depending on the geometry as well as on the deposition techniques and anneal [75], [76]. In the 3-D NAND scheme, for example, due to the constrained geometry, the grain size is of the order of nanometers [6], [76]. The transition region between two grains is called a grain boundary [77] and acts as a defect able to trap carriers. Therefore, the poly-Si conduction is dominated by scattering events at grain boundaries and at charged defects [76], [78], [79], that cause current variation and fluctuations, also known as Random Telegraph Noise (RTN) [80], leading to reliability issues. The conduction depends on both the grain size and the crystal orientation [73], [76], [78], [82]. In addition, as the number of stacked cells increases, the current will decrease, making poly-Si unsustainable for future generation of 3-D NAND.

1.3 Thesis Outline

Vertical 3-D NAND memory technology is currently in production as replacement of planar FG beyond the 15 nm node, and the industrially most relevant schemes feature poly-Si as channel material. However, the I_D required for the memory read operation is low, unstable and with a broad distribution. Furthermore, it is decreased by increasing the number of stacked layers, rendering poly-Si a showstopper for 3-D NAND.

The purpose of this doctoral thesis is to investigate alternative channel materials with electron mobility higher than poly-Si, as a possible solution to enable further stacked layers for future 3-D NAND generations. III–V semiconductors such as GaAs, InP, $In_xGa_{1-x}As$ and InAs, are attractive candidates to replace Si, thanks to their higher electron mobility [83]–[86]. However, the integration of a new channel material in 3-D NAND is not straightforward and requires the modification of some steps in the Si-based process flow, as well as the introduction of new ones.

In this work particular attention is given to the fundamentals of III-Vs integration in 3-D NAND memory and to the impact that the most challenging steps of the process integration have on the electrical performance.

In **chapter 2**, a preliminary screening of III-V materials to be integrated in 3-D geometries is conducted on 200 mm blanket wafers. III-V compounds

properties are investigated by conducting both electrical and physical characterizations. The electron mobility is extracted using standard Hall mobility measurements. Crystallinity and grain sizes are evaluated by means of several techniques and are correlated with electron mobility on samples with and without ex-situ thermal annealing.

In **chapter 3**, the main focus is on the engineering of grain size in poly-Si channels and the integration of $Si_{1-x}Ge_x$ in our single CG test vehicle. The grain sizes of poly-Si channels with different flavors are extracted with the aim to study the impact of grain sizes on the I_D. Epitaxially grown Si (Epi-Si) is also integrated and electrically evaluated to benchmark poly-Si channels. Thanks to its better compatibility with the Si-based process flow, $Si_{1-x}Ge_x$ is used as stepping stone to determine the integration challenges when poly-Si is replaced with a new channel material.

In **chapter 4**, the most challenging steps to integrate epitaxially grown $In_xGa_{1-x}As$ by Metal Organic Vapor Phase Epitaxy (MOVPE) are discussed. The epitaxial growth, the channel filling capability and its composition, are investigated by exploring different gallium (*Ga*) precursors, flow ratios and growth temperature. Furthermore, special attention is given to the surface preparation required to initiate the III-V growth and its impact on the memory stack integrity is studied through physical and electrical characterization. The conduction properties of $In_xGa_{1-x}As$ channels are also analyzed as a function of different indium (*In*) concentrations and compared with the Si-reference.

In **chapter 5,** advanced characterization is conducted on the III-V devices presented in Chapter 4. TCAD simulations are carried out to assess the impact of channel variability on the electrical performance and to find a pathway for device improvement. Based on the simulation guidelines, optimized devices are fabricated and benchmarked against epi-Si channels. Furthermore, deuterium annealing is used in the attempt to passivate the defects at the channel/TuOx interface and in the TuOx.

Finally in **chapter 6** the conclusions of the present work are summarize, and a brief outlook for future work is also reported.

Chapter 2

Exploration of III-V properties on blankets

2.1 Introduction

The device integration requires many materials to be compatible through each fabrication step, such as deposition, thermal annealing, cleanings. An easy way to assess the compatibilities issues and their impact on the materials properties is using blanket layers.

In this chapter blanket films are used to conduct a first screening of the physical and electrical properties of polycrystalline InAs, $In_xGa_{1-x}As$ and GaAs in view of their possible integration as channel materials in 3-D NAND memories. Particular attention is addressed to the investigation of the III-Vs mobility which has to be high to enable further stacked layers for future 3-D NAND generations, as well as to the thermal stability; those are important key parameters for the choice of a proper material to be used as poly-Si channel replacement in 3-D NAND.

Contrary to the CMOS technology, where the gate stack is always fabricated after the channel [87], the 3-D NAND integration flow is reverted and the gate stack is deposited prior to the channel formation, as better described in Chapters 3 and 4. Due to the different integration approaches used, the studies reported in literature on the interface quality between the III-V channels and the gate stacks [88], [89] are not necessarily applicable to our case. Therefore, in this chapter an attempt to pattern III-V blankets is done to evaluate the quality of the interface between III-V and different gates oxides, by emulating the gate first-channel last approach of our 3-D

NAND. The patterning of the blankets has also the aim to assess the contact resistances when III-Vs are contacted with metals.

2.2 Sample preparation

Polycrystalline InAs, $In_xGa_{1-x}As$ and GaAs layers are deposited by Molecular Beam Epitaxy (MBE) [90], [91] with a thickness of ~180 nm on top of a 300 nm thick SiO_2 on 200 mm Si wafers, as shown in Fig. 2.1.

To perform Hall mobility measurements the III-V layers are doped during the deposition by adding *Si* as n-type dopant, through a Si source tunable in temperature. By changing the Si source temperature, the amount of doping can be changed; for our experiments, two different Si dopant source temperatures are adopted: 1150 ˚C and 1250 ˚C.

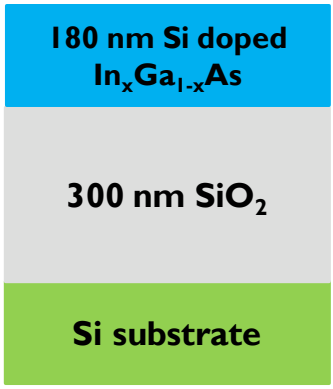


Figure 2.1: Cross-section of Si doped poly-$In_xGa_{1-x}As$ layers deposited by MBE on top of 30 nm thick SiO_2. The composition, x, ranges between 0 and 1.

In order to determine the thermal stability of the III-V layers, the samples are subjected to ex-situ rapid thermal process (RTP) at three different temperatures, namely 350 ˚C, 450 ˚C and 500 ˚C, during 10 min in Forming Gas Atmosphere (FGA) (Hydrogen(H_2): Nitrogen (N_2)=0.1). These conditions are selected as based on the results of [92].

2.3 Physical characterizations

Physical characterization is conducted in order to investigate the crystallinity and composition of our III-V compounds. Samples are analyzed by using several characterization techniques: Grazing Incidence X-Ray Diffraction (GI-XRD) is used to obtain information on the crystal orientation, composition and grain size. Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) analysis give information on the material topography (e.g., grain size, defectivity, presence of voids). The elemental analysis is conducted by Rutherford Backscattering Spectrometry (RBS) and Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS).

2.3.1 GI-XRD analysis

GI-XRD is a non-destructive technique that reveals information about the crystalline structure of the materials [93]–[95]. GI-XRD measurement is performed at a constant angle of incidence, ω, of the X-rays, where only the detector is moved over a 2θ range of interest, as shown in Fig. 2.2.

The X-ray diffraction occurs in a crystal when parallel X-rays, with a wavelength (λ) comparable to the atomic spacing, are scattered in a specular way by the atoms of a crystalline system and interfere constructively. The condition to have a constructive interference is shown in Fig. 2.3: the difference between the path lengths *ABC* and *A'B'C'* of the two waves is equal to an integer multiple of λ. The path difference between two waves undergoing constructive interference is given by Bragg's law [96], [97]:

$$n\lambda = 2d_{hkl}sin\theta \ , \tag{2.1}$$

where n is a positive integer number indicating the order of the radiation, θ is the incident Bragg angle and d_{hkl} is the interplanar spacing in a crystal, as sketched in Fig. 2.3.

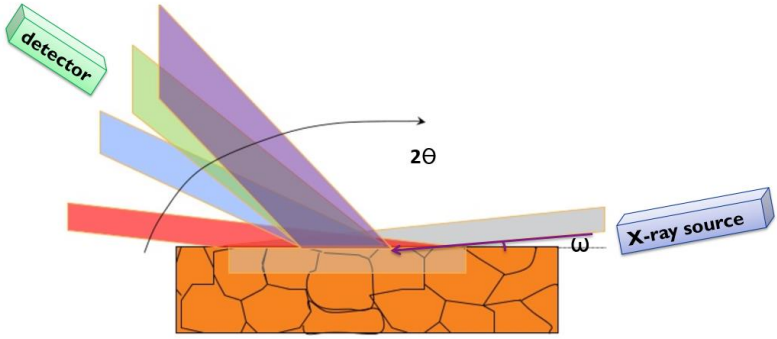


Figure 2.2: Schematic of GI-XRD geometry. GI-XRD is performed at a constant angle of incidence, ω, and the detector is moved over a 2θ range of interest [94].

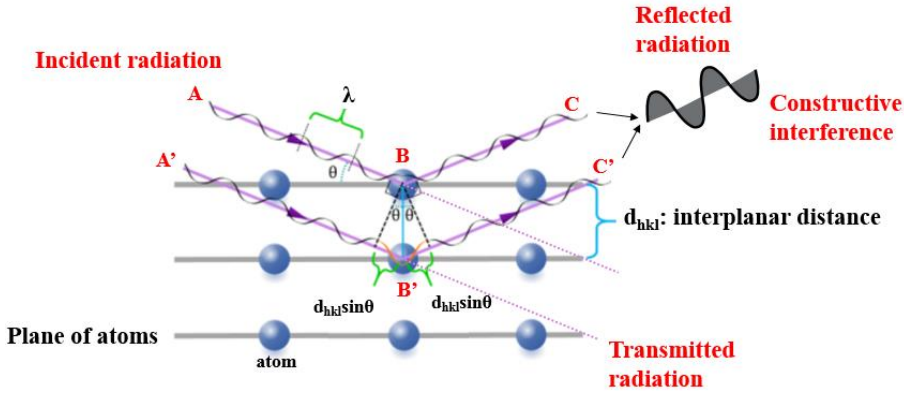


Figure 2.3: Sketch describing the Bragg diffraction. Two beams with identical wavelength and phase approach a crystal and are scattered by the atoms. The lower beam traverses an extra length of $2dsin\theta$ which is an integer multiple of λ, generating a constructive interference.

The pattern generated by the diffracted X-rays beam is called diffractogram (Fig. 2.4) and it is formed by maxima (or peaks) with different intensities. The intensity of the peaks is proportional to the electronic density of the crystallographic planes that form the crystal. The position of the peaks depends on the interplanar distance d_{hkl}, as given by the Bragg condition, and corresponds to a different plane orientation

described by using the Miller indexes *hkl* notation [98], [99]. For each crystalline ordering, the diffractogram is unique and therefore it is a finger print of the analyzed sample.

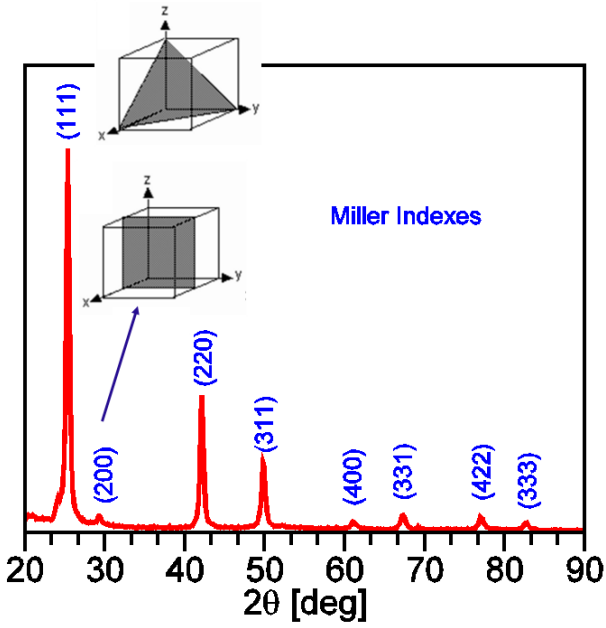


Figure 2.4: XRD diffractogram of poly-InAs layer. The *2θ* scan is done in range between 20º and 90º. Miller indexes are used to describe the different crystallographic plane orientations; the sketches of the (111) and (200) planes are reported as example.

The relationship between d_{hkl}, Miller indices, *hkl*, and the lattice constant *a* for a cubic crystal system is given by [98], [100]:

$$a = d_{hkl}\sqrt{(h^2 + k^2 + l^2)} \quad , \tag{2.2}$$

d_{hkl} is determined by using Eq. (2.1), while the Miller indices (*hkl*) of the Bragg planes are considered as the ones given in the powder diffraction file of the Inorganic Crystal Structure Database for the III-V layers [101].

Once *a* is calculated, the extraction of the *In* content ([*In*]) in our $In_xGa_{1-x}As$ layers can be done by using the Vegard's law [102]; it is an empirical relationship which states that a linear relation exists between the

lattice parameter of an alloy and the concentration of its constituents [102], given by Eq. (2.3) as:

$$a_{InGaAs} = x a_{InAs} + (1 - x) a_{GaAs} \ , \tag{2.3}$$

where a_{InGaAs}, a_{GaAs} and a_{InAs} are the lattice parameters of $In_xGa_{1-x}As$, GaAs (5.65 Å) and InAs (6.06 Å) [103], respectively. The a_{InGaAs} is a value in between the ones of GaAs and InAs, and it is a function of the composition [103].

The average size of the crystallites that form the sample can be estimated from the broadening of the XRD reflections by means of the so-called Scherrer's formula [104]:

$$\tau = \frac{K\lambda}{\beta cos(\theta)} \ , \tag{2.4}$$

where τ is the crystallite size (CS), K is a dimensionless shape factor (assumed equal to 1), β is the full width at half maximum (FWHM), as depicted in Fig. 2.5.b. The final values of the CSs are reported in this thesis with the name of in-plane grain size (GS) and they are an average result obtained for the three peaks with the highest intensities observed in the diffractogram (Fig. 2.5.a); each peak is first filtered to remove the noise floor and then is fitted with a Lorentzian profile [105], as shown in Figs. 2.5.(b-d), by using the software Origin [106]. The resolution of the diffractometer used is ~5 nm, meaning that this is the minimum CS that can be measured by our X-Ray diffraction setup.

The measurements are performed in a Jordan Valley *Bede Metrix*^{TM}*-L* apparatus, keeping the angle of incidence ω of the X-ray beam (CuKα radiation, λ = 0.15418 nm) at 1º. The tool is equipped with the *Bede Control* software for data acquisition. The software *Origin* is used for data analysis.

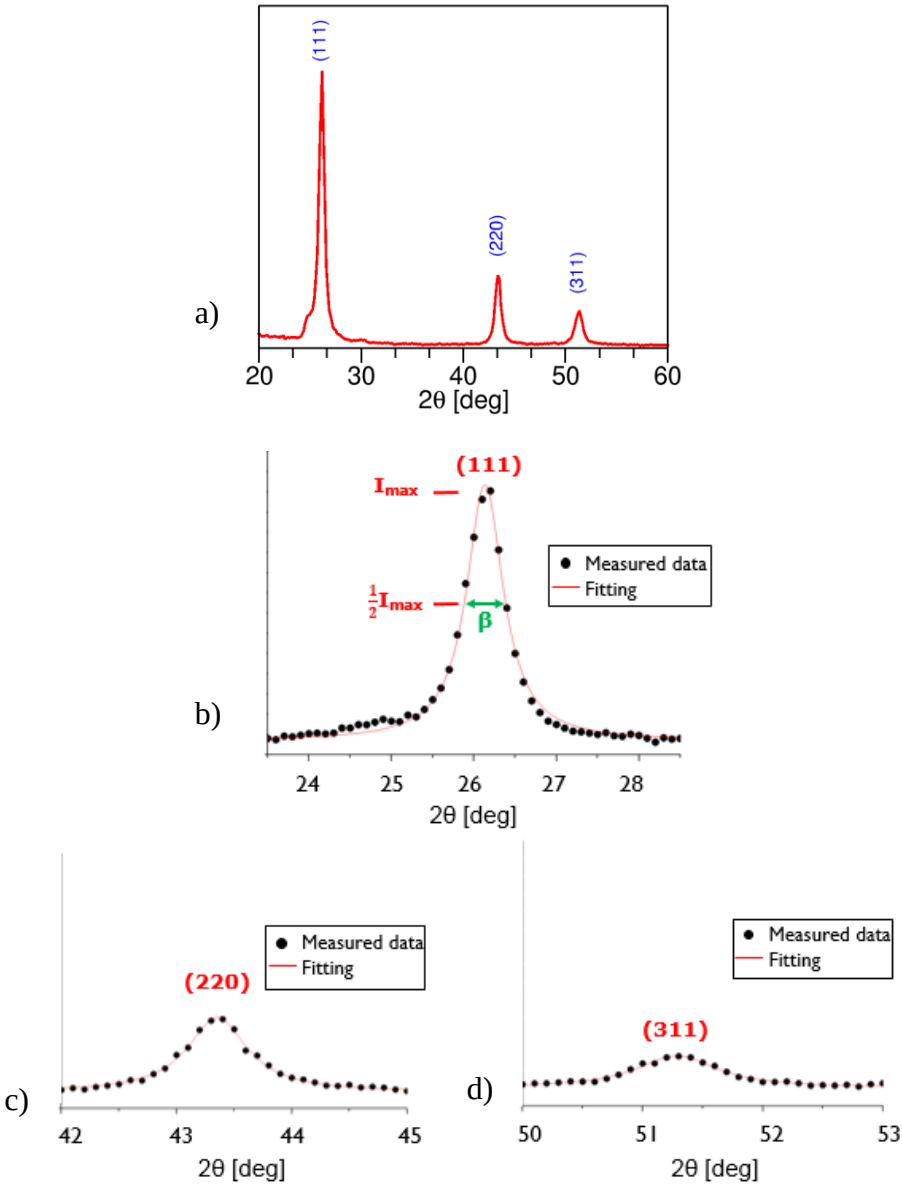


Figure 2.5: a) Diffractogram of a $In_xGa_{1-x}As$ layer using 1150 ˚C as *Si* source temperature. b, c, d) The three available reflections are first filtered to remove the "floor noise" and fitted with Lorentzian profiles for the extraction of the CS.

2.3.2 Top-Down-SEM inspections

Top-Down-SEM (TD-SEM) analysis is conducted in order to extract the out-plane GS in our III-V layers.

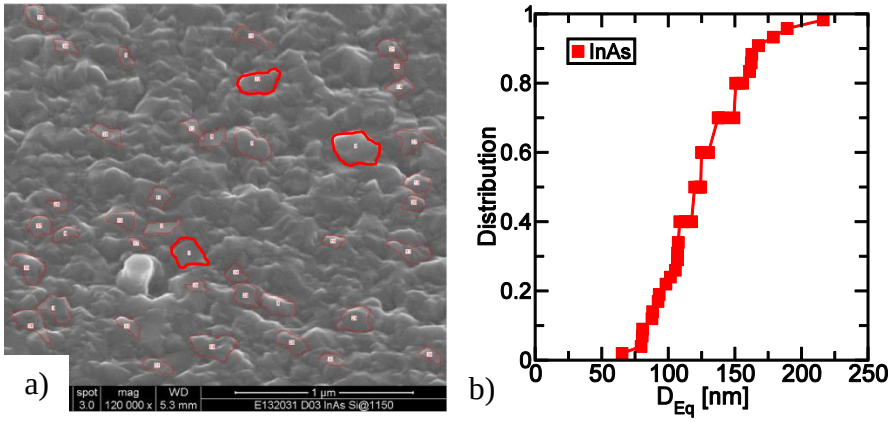


Figure 2.6: a) TD-SEM of InAs prepared using 1150 ˚C as *Si* source temperature; clearly visible grains are seen (see e.g., red markers). b) Distribution of the extracted D_{EQ} of ~35 grains on a sample of 2x2 µm^2.

Images are processed with the software "ImageJ" [107], [108]. First of all the spatial scale has to be defined to calibrate the desired measurement unit; the straight line selection tool is used to select the line that corresponds to a known distance in the TD-SEM image (e.g., 1 µm in the image shown in Fig. 2.6.a). Based on the reference length of the line selection, the distance is automatically displayed in pixels. Next, by tuning the contrast of the images, all the grains that are clearly defined are marked, as shown in Fig. 2.6.a and then processed.

The GS extracted by TD-SEM images is defined as out-plane GS and, for a certain grain, it is reported as the equivalent diameter (D_{EQ}) of a circular grain having the same area as the grain studied by using the Eq. (2.5):

$$D_{EQ} = 2\sqrt{\frac{A_{circle}}{\pi}}\ , \tag{2.5}$$

where A_{circle} is the area of the marked grain measured with ImageJ.

Figure 2.6.b shows an example of the statistical distribution of all the out-plane GSs extracted on a sample of InAs prepared using 1150 ˚C as *Si* source temperature.

2.4 Electrical characterization

Electrical characterization is performed by using the Van der Pauw sample setup and Hall mobility measurements [109], [110]; the first technique is used to extract the sheet resistance (R_s), while Hall Effect measurement is performed for the extraction of the sheet carrier density (n_s for *n*-type and or p_s, for *p*-type material). The mobility (μ) is evaluated by combining R_s, and n_s or p_s results.

For the electrical characterization, samples of 1x1 cm^2 are cut. Then, the contacts are created by putting *In* dots on the four corners of each square sample and by applying a bake at 270 ˚C for 30 sec in FGA. Afterwards, a first assessment of the contact quality is done by measuring the contact resistance with a multimeter.

There are many aspects which influence the accuracy of the final electrical results, such as: the quality of the contacts created on the sample, the homogeneity, the symmetry of the sample and the power dissipation during the measurements, which has to be kept lower than 5 mW [109], [110].

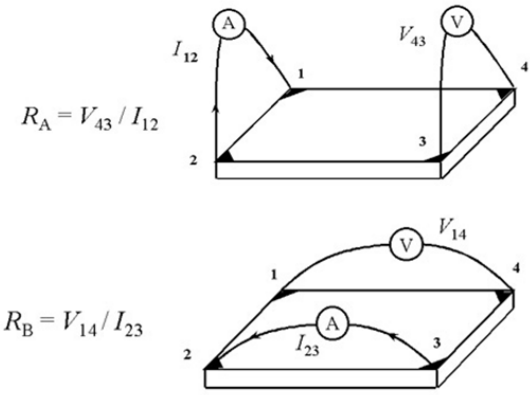


Figure 2.7: Setup to determine the characteristic resistances R_A and R_B in a rectangular sample [109].

Figure 2.7 shows the setup used to determine the R_s and to control as well the quality of the Ohmic contacts [111], via the measurements of the *I-V* linearity between neighboring contacts; a constant direct current I_{12} is applied between terminals 1 and 2, while a voltage V_{43} is measured between terminals 4 and 3. Afterwards, the polarity of the current is reversed (I_{21}) and V_{34} is measured. The measurements are repeated to obtain the following values of voltage V_{41}, V_{14}, V_{12}, V_{21}, V_{23}, V_{32}. From the eight measurements of voltage, eight values of resistance are obtained as follows:

$$R_{12,43} = \frac{V_{43}}{I_{12}} \qquad R_{21,34} = \frac{V_{34}}{I_{21}} \ , \tag{2.6}$$

$$R_{23,14} = \frac{V_{14}}{I_{23}} \qquad R_{32,41} = \frac{V_{41}}{I_{32}} \ , \tag{2.7}$$

$$R_{34,21} = \frac{V_{21}}{I_{34}} \qquad R_{43,12} = \frac{V_{12}}{I_{43}} \ , \tag{2.8}$$

$$R_{14,23} = \frac{V_{23}}{I_{14}} \qquad R_{41,32} = \frac{V_{32}}{I_{41}} \tag{2.9}$$

The measurement consistency per current reversal requires that:

$$R_{21,34} = R_{12,43} \qquad R_{32,41} = R_{23,14} \ , \tag{2.10}$$

$$R_{43,12} = R_{34,21} \qquad R_{14,23} = R_{41,32} \tag{2.11}$$

The reciprocity theorem requires that:

$$R_{21,34} + R_{12,43} = R_{43,12} + R_{34,21} \ , \tag{2.12}$$

$$R_{32,41} + R_{23,14} = R_{14,23} + R_{41,32} \tag{2.13}$$

Therefore, the second half of the Eqs. (2.6)-(2.9) are redundant, allowing to check the Ohmic contact quality, the errors generated by sample non uniformity and the measurement repeatability; if any of these equalities fails to be within 3%, then the Ohmic contacts are considered to be not adequate for Van der Pauw measurements [109].

A typical *I-V* measurement of our poly-InAs samples displaying the Ohmic characteristic is shown in Fig. 2.8. The range of currents applied is

between -1 mA and 1 mA; linear characteristics are observed and, in agreement with the Eq. (2.12) and Eq. (2.13), some curves are overlapped, proving sample uniformity and measurements repeatability.

To ensure a power dissipation much lower than 5 mW, as the technique requires, the value of the current chosen for the R_s extraction, as well as for Hall mobility measurements, is 0.5 mA.

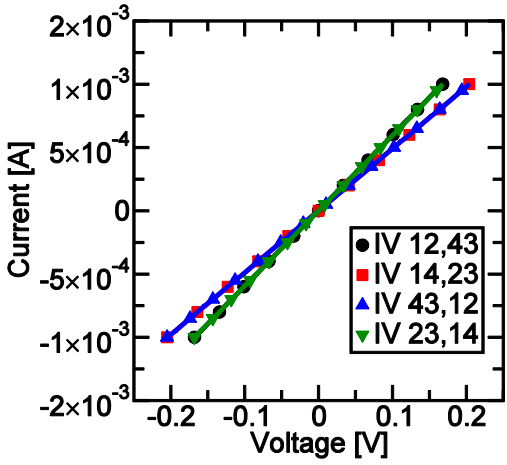


Figure 2.8: Typical I-V measurements on a poly-InAs sample, by applying the currents on different terminals. Linear characteristics are observed.

Finally, the R_S can be determined from the two characteristic resistances:

$$R_A = \frac{R_{21,34} + R_{12,43} + R_{43,12} + R_{34,21}}{4} , \tag{2.14}$$

$$R_B = \frac{R_{32,41} + R_{23,14} + R_{14,23} + R_{41,32}}{4} , \tag{2.15}$$

by using the Van der Pauw Eq. (2.16), which can be solved numerically for R_S:

$$e^{\left(-\pi * \frac{R_A}{R_S}\right)} + e^{\left(-\pi * \frac{R_B}{R_S}\right)} = 1 \tag{2.16}$$

The sheet carrier density n_s or p_s of the samples is measured using the same equipment but activating an electromagnet to generate a magnetic

force perpendicular to the samples surface in order to induce the Hall Effect in the layers of interest [109], [110].

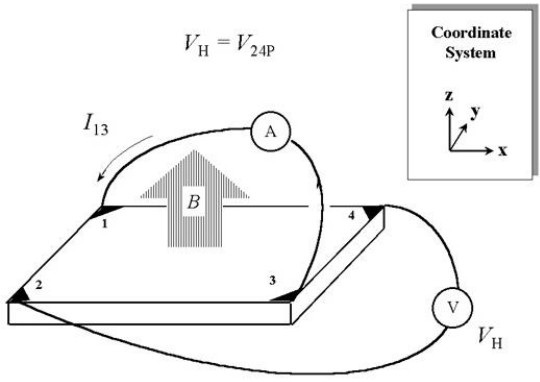


Figure 2.9: Setup to determine the Hall Voltages V_H in a rectangular sample [109].

The setup used for these measurements is shown in Fig. 2.9; first a positive magnetic field (*B*) of 152 mT is applied perpendicular to the plane of the sample, while a constant current is applied between terminals 1 and 3 (I_{13}). As already mentioned above, the value of current is 0.5 mA for all the available samples. Then, the Hall voltage V_H, is measured between terminal 2 and 4. The measurements are repeated to obtain the following values of V_H: V_{42}, V_{13}, V_{31}. Next, *B* is reversed, and the measurements described above are conducted again. The type of carriers (*n* or *p*) and the n_s or p_s are determined by the positive or negative sign using the Eq. (2.17), where *q* is the elementary charge unit (1.602×10^{-19} C):

$$n_S \; or \; p_S = I * \frac{B}{q*|V_H|} \tag{2.17}$$

Finally, the Hall mobility is determined according to Eq. (2.18):

$$\mu = \frac{|V_H|}{R_S*I*B} = \frac{1}{q*n_S*R_S} \tag{2.18}$$

The equipment used for the Van der Pauw Technique and the Hall Effect measurements is a DC power supply SM 1500 Series of Delta Elecktronika, a CENCO Physics electromagnet, a Ohmic contacting sample holder of the same company and a high input impedance voltmeter Keithley 2000. The

software used to drive the measurements and for data extraction is LabVIEW [112].

2.4.1 Physical and electrical results

As-deposited III-V layers

The samples containing GaAs show high contact resistance (>> MΩ) with variation in currents in the range of $1x10^{-8}$ to $1x10^{-2}$A. As reported in the literature [113]–[115], the oxidation of GaAs, once it is exposed to air, results in the formation of As excess and oxides such as Ga_2O_3 and As_2O_3. Ga_2O_3 represents one of the most stable Ga-oxides and it is difficult to be removed. The development of As-Ga-O native oxide can be one of the main causes of the high contact resistance, which impede further electrical characterizations. Therefore, this section will focus only on the results collected on Si-doped $In_xGa_{1-x}As$ and InAs.

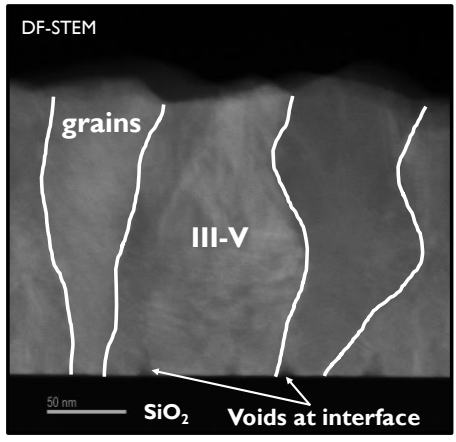


Figure 2.10: DF-STEM of 180-nm-thick poly-$In_{0.63}Ga_{0.37}As$ with *Si* source temperature of 1150 ˚C.

Figure 2.10 reports the Dark Field Scanning TEM (DF-STEM) image of 180 nm thick poly $In_xGa_{1-x}As$ with Si source temperature of 1150 ˚C; the III-V layer is composed of columnar grains and shows areas with darker contrast at the interface with SiO_2, which can be voids originated during the

deposition. The same crystallographic structure is observed in the samples with higher Si source temperature (not shown).

The physical properties of the as-deposited poly $In_xGa_{1-x}As$ and InAs films are summarized in Table 2.1.

The lattice parameters "*a*" of InAs, extracted through Eq. (2.2), are comparable to what is reported in the literature [116]. As expected, $In_xGa_{1-x}As$ presents a value of "*a*" in between the one of the InAs and GaAs (5.65 Å) alloys.

The relative amount of *In* and *Ga* are quantified using Eq. (2.3) and it is estimated around 63% of *In* and 37% of *Ga*; these values are corroborated by RBS analysis.

Recipe Name	***Si* source [°C]**	**Physical characterization**					
		<*a*> [Å]	**Composition x by XRD**	**Relative [*Si*] by RBS**	***Si* signal by ToF-SIMS [arb. unit]**	**In-plane <GS> [nm]**	**Out-Plane <GS> [nm]**
$In_xG_{1-x}As$	1150	5.91 (1)	0.63	< 1.3 at%	0.4	14	100
	1250				4.2	15	
InAs	1150	6.07 (1)	1		2.1	20	130
	1250				14.9	19	100

Table 2.1: Physical properties of as-deposited $In_xGa_{1-x}As$ and InAs films.

The *Si* dopant concentration is found to be less than 1.3 at % by RBS. Moreover, ToF-SIMS analysis, of which some results are illustrated in Fig. 2.11, shows that the level of Si-content is enhanced by increasing the Si-source temperature for both $In_xGa_{1-x}As$ and InAs layers.

The *Si*-doping temperature does not affect the composition and the GS of the III-V layers, as shown in Fig. 2.12.

The in-plane <GS>, extracted by using Scherrer's formula (Eq. (2.4)) are comparable over the layers of the same compositions and different *Si* source temperatures (Table 2.1). This is also valid for the out-plane <GS> extracted from the TD-SEM images on $In_xGa_{1-x}As$ layers. InAs combined with lower Si source temperature shows instead a slightly larger out-plane <GS>, as seen in Table 2.1.

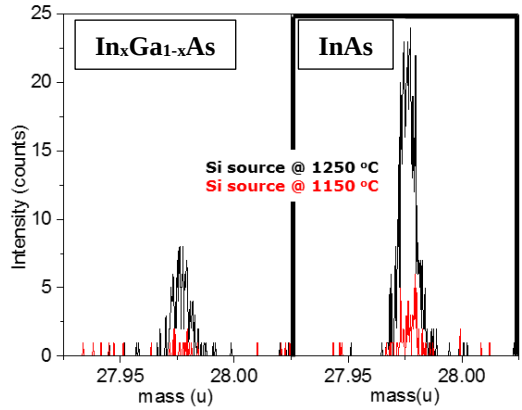


Figure 2.11: $^{28}Si^-$ signals measured on $In_xGa_{1-x}As$ and InAs films by ToF-SIMS. Indicated Si temperatures correspond to the *Si*-source temperature used during MBE deposition.

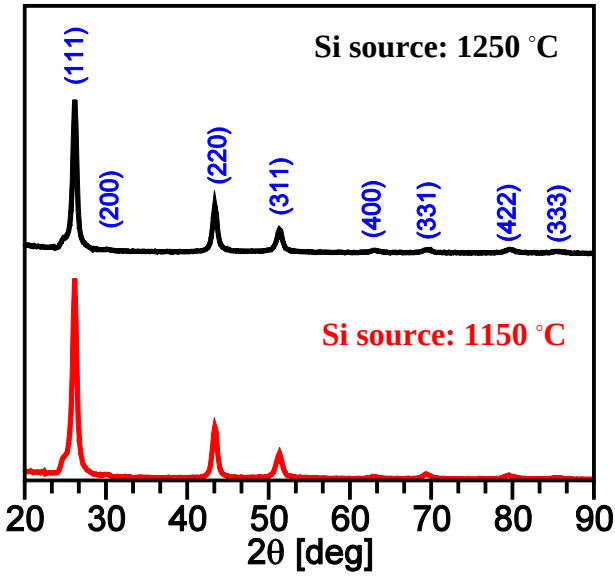


Figure 2.12: Diffractograms of $In_xGa_{1-x}As$ layers doped with *Si* source at different temperatures. Comparable results are observed.

Figure 2.13 shows the SEM inspections conducted on InAs using 1150 ˚C and 1250 ˚C as *Si* source temperature. The sample with lower *Si*

source temperature (Fig. 2.13.a) is rougher, compromising a proper evaluation of the out-plane GS; it will result in an overestimated value, as shown in Fig. 2.14.

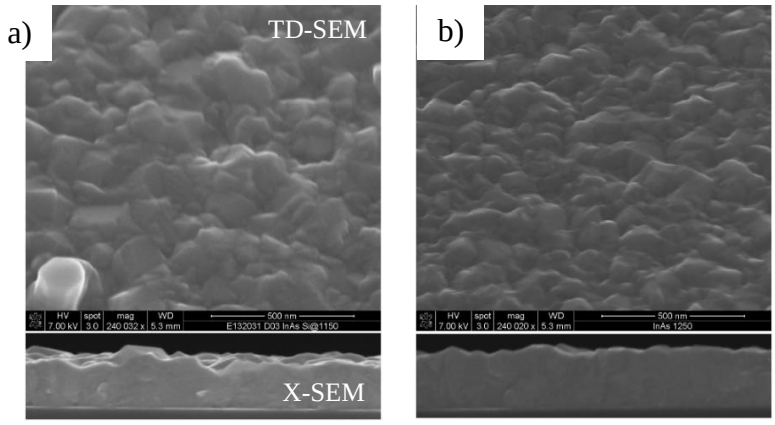


Figure 2.13: TD-SEM and X-SEM of a) InAs using 1150 ˚C as *Si* source temperature and b) InAs using 1250 ˚C as *Si* source temperature.

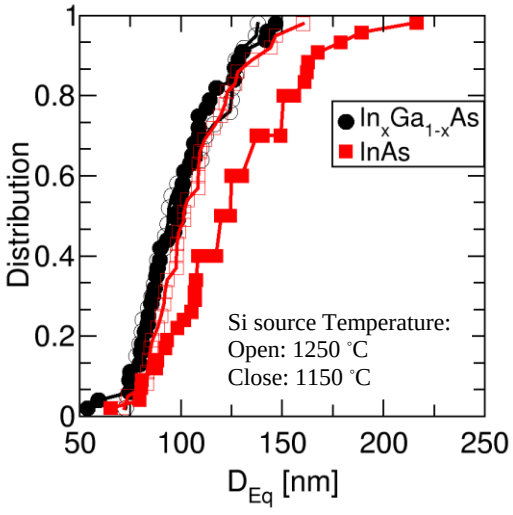


Figure 2.14: In-plane GS for $In_xGa_{1-x}As$ and InAs samples extracted by using TD-SEMs views. The values extracted for InAs using 1150 ˚C as *Si* source temperature are overestimated due to the roughness of the III-V layer.

Recipe Name	Si source [°C]	Electrical characterization		
		R_s [KΩ/Sq]	n_s [cm^{-2}]	μ [cm^2/Vs]
$In_xG_{1-x}As$	1150	33	2.7×10^{12}	52
	1250	17	1.5×10^{13}	23
InAs	1150	0.3	4.8×10^{13}	432
	1250	0.2	2.1×10^{14}	138

Table 2.2: Electrical properties of as-deposited $In_xGa_{1-x}As$ and InAs.

Table 2.2 summarizes the electrical characterization results. As expected, poly-InAs, has a lower R_s (by a factor 100) and higher μ (by a factor 10) than $In_xGa_{1-x}As$. This result originates from the intrinsic properties of InAs, such as the low band gap (0.35 eV against the 0.65 eV for $In_xGa_{1-x}As$ with x around 63% [116]), which makes such compound less resistive and with better μ [117], [83]. Both the R_s and the μ decrease as the n_s increase. These behaviours are in line with what is reported in the literature [118], [119]. The n_s in turn decreases with decreasing the temperature of the *Si* dopant source, and it is lower in the $In_xGa_{1-x}As$ films, corroborating the ToF-SIMS results (Table 2.1).

III-V layers after ex-situ annealing

Fig. 2.16 shows the diffractograms of $In_xGa_{1-x}As$ layers doped at 1150 °C, before and after ex-situ annealing conducted at temperatures ranging between 350 °C and 500 °C in FGA. Table 2.3 and 2.4 summarize the physical and the electrical results upon annealing for $In_xGa_{1-x}As$ and InAs, respectively.

Independent of the Si source temperature, $In_xGa_{1-x}As$ can be considered thermally stable in terms of composition, since the peak positions in the diffractograms do not display any evident variation among all the samples studied (Fig. 2.15). This result is also valid for InAs samples (not shown). On the other hand, the FWHM of the peaks can change, indicating that the in-plane GS is affected by the annealing. A slight GS enlargement is observed in InAs samples (see Table 2.4), while no GS variation is observed in $In_xGa_{1-x}As$ samples, as summarized in Table 2.3.

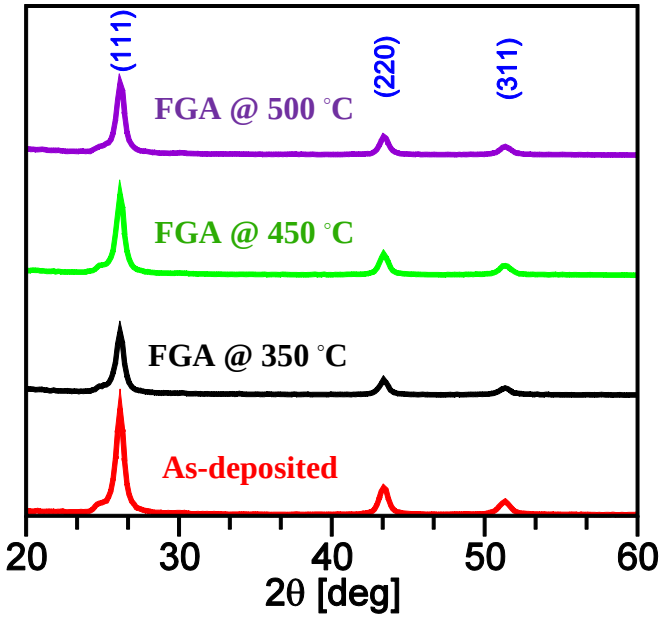


Figure 2.15: Diffractograms of $In_xGa_{1-x}As$ layers using Si source temperature of 1150 ˚C after ex-situ annealing in FGA at different temperatures. The results are comparable.

	$In_xGa_{1-x}As$ Si Source temperature: 1150 ˚C				**$In_xGa_{1-x}As$ Si Source temperature: 1250 ˚C**			
RTP [˚C]	**n_s 10^{12} cm^{-2}**	**R_s [KΩ/Sq]**	**μ [cm^2/Vs]**	**GS [nm]**	**n_s 10^{13} cm^{-2}**	**R_s [KΩ/Sq]**	**μ [cm^2/Vs]**	**GS [nm]**
350	4.6	28	48	15	1.7	16	23	15
450	6.4	12	81	14	2.1	8	36	16
500	7.4	11	79	15	2.3	7	38	16

Table 2.3: Physical and electrical properties of $In_xGa_{1-x}As$ upon ex-situ FGA anneal. The GS refers to the in-plane <GS> extracted by Eq. (2.4).

In $In_xGa_{1-x}As$ layers the thermal treatments help to activate more Si-doping, as suggested by the slight n_s increase, with a consequent decrease of the *Rs* (Table 2.3). However, the *Rs* reduction appears relatively more significant as compared to the small n_s variation and may be related, as well, to a reduction of defects at the grain boundaries and/or in the grains upon annealing in FGA. Furthermore a mobility increment of ~65% is observed

when the annealing temperature is increased and independently of the used Si source temperature. Nonetheless, the increment of μ tends to a limit value of around 81 cm^2/Vs and 38 cm^2/Vs for $In_xGa_{1-x}As$ doped at 1150 ˚C and 1250 ˚C, respectively (Table 2.3). Such behavior may be caused by the tendency of the R_s to reach a minimum value at high temperatures whilst the n_s tends to increase with temperature, as summarized in the Table 2.3.

	InAs Si Source temperature: 1150 ˚C				**InAs Si Source temperature: 1250 ˚C**			
RTP [˚C]	**n_s 10^{13} cm^{-2}**	**R_s [KΩ/Sq]**	**μ [cm^2/Vs]**	**GS [nm]**	**n_s 10^{14} cm^{-2}**	**R_s [KΩ/Sq]**	**μ [cm^2/Vs]**	**GS [nm]**
350	5.4	0.27	431	20	2.7	0.14	162	19
450	6.3	0.18	557	22	2.3	0.13	207	21
500	4.7	0.21	634	24	2.0	0.09	333	22

Table 2.4: Physical and electrical properties of InAs upon ex-situ FGA anneal. The GS refers to the in-plane <GS> extracted by Eq. (2.4).

Similarly to the $In_xGa_{1-x}As$ case, the μ in InAs layers increases by ~50% with the RTP (Table 2.4). The μ enhancement coincides with a slight reduction of n_s and R_s in the same proportion, when the anneal temperature is increased, as summarized in Table 2.4. This reduction may be thus related to the ~20% of GS enlargement, as measured by XRD.

2.5 Patterning of blankets for in-depth electrical characterization

Large capacitor-like and thin-film-transistor (TFT)-like simplified structures are fabricated by using a reverse flow (gate first approach) through both lift-off an etching techniques [120], as described in the following sub-paragraphs. The patterning of blankets has the aim of:

- electrically characterizing the interface between III-V and oxides, such as SiO_2 and aluminum oxide (Al_2O_3), and extracting information on the trap density, in order to optimize the interface in view of the integration in the 3-D vehicle.

- evaluating the contact resistance with metals, in view of metal drain formation in the integrated 3-D vehicle (as will be discussed in Chapter 4).

2.5.1 Experimental Setup

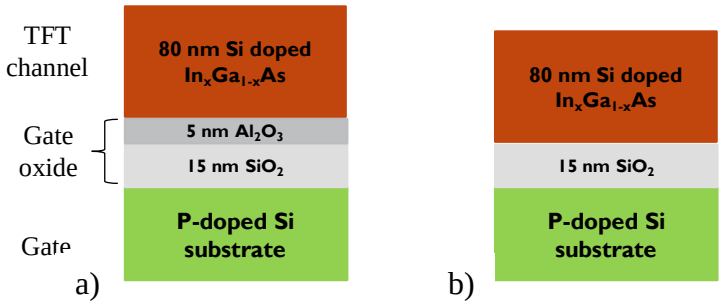


Figure 2.16: Cross-sections of *Si* doped poly-$In_xGa_{1-x}As$ layers deposited by MBE on top of a) 5 nm Al_2O_3 and b) 15 nm SiO_2. The indicated values of the thicknesses are nominal.

Fig. 2.16 shows the cross-sections of the 200 mm blanket wafers used for the fabrication of capacitors and TFTs by a gate-first approach; *Si* substrate is doped with phosphorus (*P*), in order to be used as gate or bottom contact; *P* is implanted in a dose of $3x10^{15}$ cm^{-2} and with an energy of 8 KeV. Then, the dopant is activated at 1050 ˚C in N_2 atmosphere for 2 min. Poly-$In_xGa_{1-x}As$ layers are deposited with a nominal thickness of 80 nm by MBE on top of either 5 nm thick Al_2O_3, which in turn is deposited on SiO_2, or on 15 nm thick SiO_2. Al_2O_3 is deposited by ALD, while the SiO_2 is created by oxidation of the substrate.

The patterning process is conducted on samples of 5x5 cm^2 size either via lift-off lithography or employing a chemical etching [120]. In the first case, illustrated in Fig. 2.17.a, after cleaning in acetone and isopropyl alcohol (IPA) (1), the surface is spin-coated with a photo-resist (PR) material (2). Then, the sample is exposed to ultra violet (UV) light in order to transfer the pattern present on the used dark field (DF) mask to the surface (3). The part of PR which has reacted during the exposure is then removed through a development of the PR film (4). In step (5), the metal stack is deposited; it consists of 30 nm thick molybdenum (*Mo*), which is the layer in contact with III-V, and 50 nm thick aluminum (*Al*). Finally solvent-based

chemicals are used to dissolve the remaining PR and the metal layer on top of it, leaving the metal only in the region of interest (6).

In the second approach (see Fig. 2.17.b), the metal is deposited just after the III-V cleaning (step (1)) on top of the whole surface (2). In the step (3) PR is deposited and the surface is exposed to UV through a light field (LF) mask onto which the pattern is present (3). The reacted PR is instead removed in step (4). Afterwards the metal layer needs to be etched away from the areas where it is not covered by the PR layer (5). In our experiments some samples were also subjected to etching of III-V layer by using a sulfuric-based chemistry (5), to better isolate the structures of interest from each other's. Finally step (6) follows, similar as described for the lift-off approach.

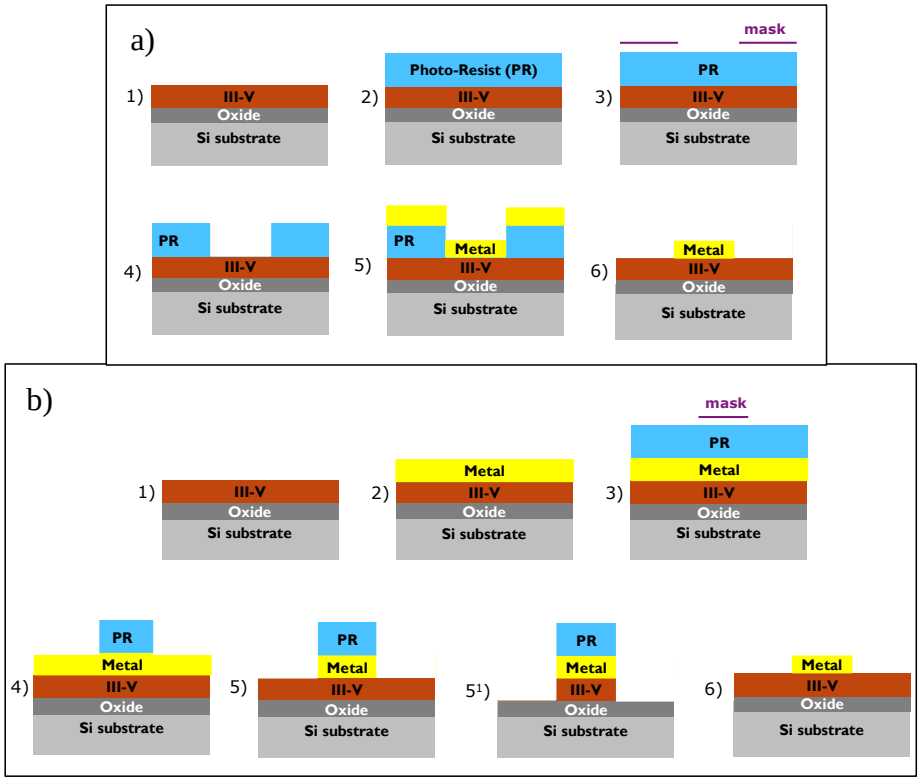


Figure 2.17: Schematic illustration of a) lift-off and b) etching process flows.

The choice to use lift-off or chemical etch approach depends mostly on the possibility and the easiness of etching the metal and the III-V surface in a selective way so that it does not harm the stack of layers to be patterned.

Figure 2.18 shows a schematic representation of the structures used for the fabrication of the capacitors and transistors, and the final sketch of both the manufactured capacitor and TFT. The dark areas (in violet) represent the metal contacts. Furthermore, circular metal pads of equal size (R_{in}) are separated by a ring-shaped gap with different sizes L (from 1 µm up to 32 µm); the circular metal pads with radius R_{in} serve as Source and the rest of the metallic surface is used as Drain contact.

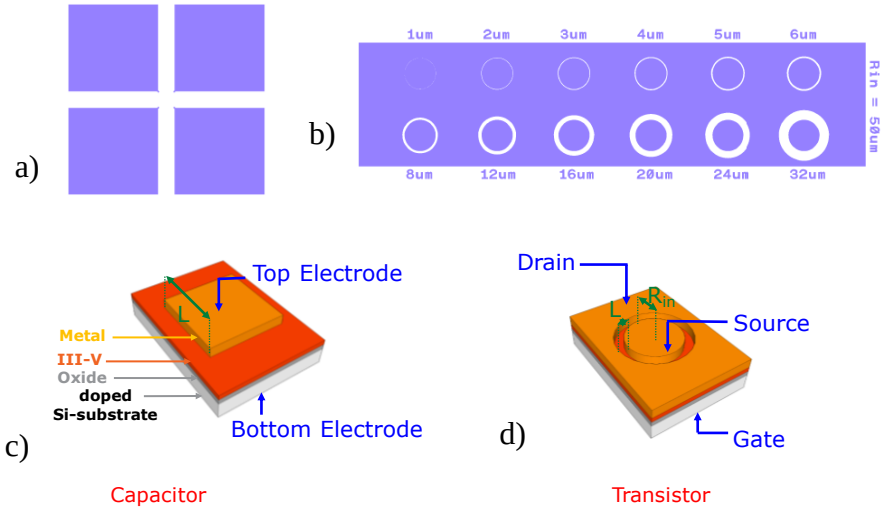


Figure 2.18: Schematic representation of a) capacitors and b) structures normally used for the Circular Transmission Line Model (CTLM) [121], as reported in the layout of the used mask. c) Sketch of the final capacitor; the metal left after etching is used as Top Electrode, while the substrate represents the Bottom one. d) Sketch of the final transistor by using CTLM structures.

2.5.2 Results on patterned samples

Figure 2.19 shows the profile of metal on structures normally used for the extraction of the contact resistance via the CTLM [121], after both

lift-off and metal etching by using a Bruker Dektak XT contact profilometer; the metal film thickness is measured by sensing the deflection of a fine stylus that is raster scanning over the surface. The nominal thickness of the metal stack is 80 nm (30 nm *Mo*/50 nm *Al*), while the measured one is ~70 nm (Fig 2.19). Furthermore, the lift-off approach seems more reliable than the metal etch, which in turn results in larger ring shaped gaps than the nominal values, as result of a lateral etch [120].

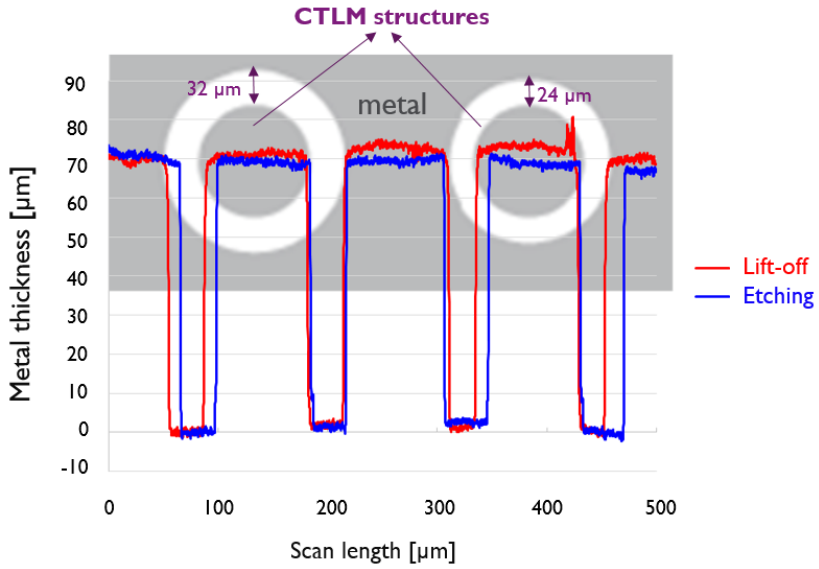


Figure 2.19: Profile of the top metal on CTLM structure after lift-off and metal etch. The circular metal pads have the same nominal size R_{in} = 50 µm and are separated by a ring-shaped gap with nominal sizes L of 32 µm and 24 µm.

After the fabrication, a gate leakage (I_G) check between the Source and the Gate is conducted on the TFT, in order to make sure that the devices are properly working; I_G-V_G characterization is conducted by sweeping the Si-substrate, which serves as gate, from -5V up to 5V, and grounding the source, (see Fig. 2.18.c for the TFT sketch). The I_G should be negligible (~0 A), as the gate is isolated by the oxide. In our case instead, independently of the technique used for the device fabrication, the I_G increases linearly with the gate voltage, indicating the presence of a leakage

current through the oxide; capacitors also behave like resistors, as shown in Fig. 2.20.

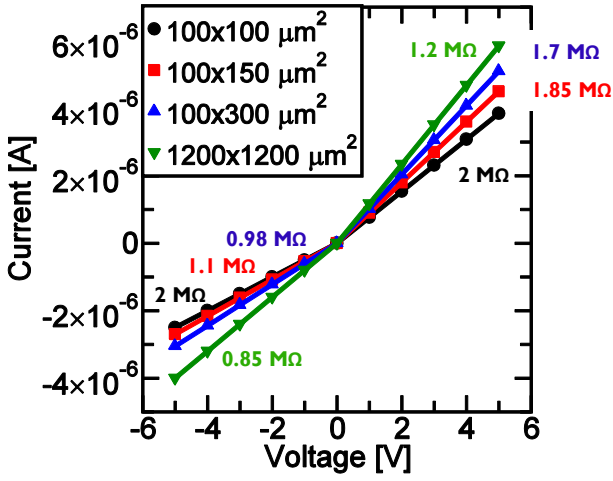


Figure 2.20: Resistance measured between Top and Bottom electrodes of capacitors with different dimensions, fabricated by etching process.

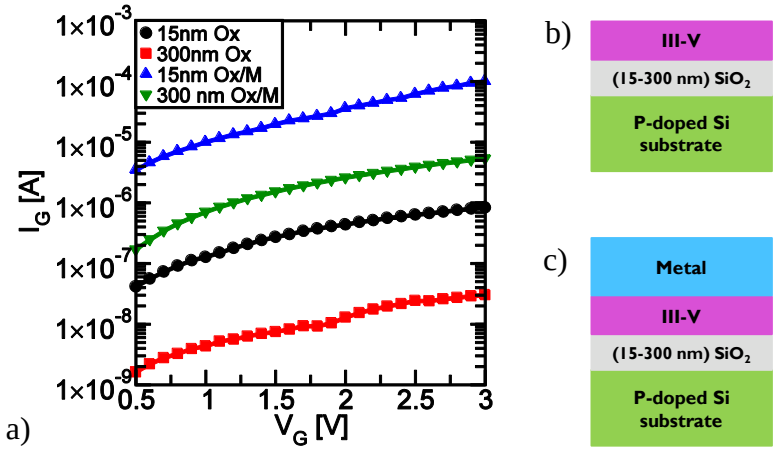


Figure 2.21: a) I_G-V_G characterization on un-patterned samples. b) Sketch of measured blankets contacting directly the III-V layer. c) Sketch of measured blankets after metal deposition. Two different SiO_2 thicknesses are tested: 15 nm and 300 nm. The leakage increases for thinner SiO_2 and after depositing the metal on top of the III-V layer.

The leakage through the oxide can be caused by several factors such as damaging of the sample due to the patterning, too thin oxides, or inter-diffusion of metal.

To exclude possible damaging that might result from patterning, I_G-V_G are also performed on un-patterned samples with and without metal, and with two different thicknesses of the oxides (15 nm and 300 nm). The results are shown in Fig. 2.21: the leakage increases by reducing the oxide thicknesses and by depositing the metal layer. The introduction of metal is creating a leakage path even in the presence of a thicker SiO_2.

X-SEM inspection, reported in Fig. 2.22, does not show any evident damage that can be considered as the cause of the leakage observed.

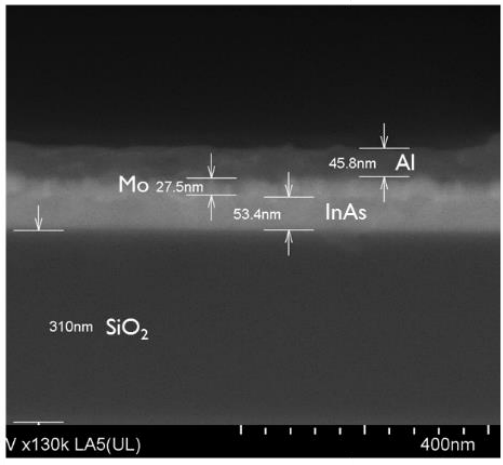


Figure 2.22: X-SEM inspection on an un-patterned sample. The stack is characterized, from bottom to top, as: SiO_2/InAs/Mo/Al. The thickness of the III-V layer is ~50 nm, against the nominal 80 nm, while the metal stack thickness is in line with the one measured by the profilometer (Fig. 2.19).

The leakage path may be intrinsically related to the used fabrication route. Indeed, both the available lift-off and the etching processes flows are not optimized to etch rough layers as our polycrystalline III-V, but are normally used on smooth surfaces such as epitaxially grown layers. The roughness of the films plays an important role not only in the etching rate variation but especially in the effectiveness of the cleanings used for the

residues removal. The etching process on rough surfaces is more complicated than the expectations and requires an intensive study of the cleanings steps and a lot of resources to conduct such investigation. The tuning of the etching process on blankets goes beyond the final scope of this thesis to integrate alternative channel materials on a constrained geometry such as 3-D NAND. Therefore, the investigation of both the interface and the metal contact is moved directly to our in-house 3-D NAND test vehicle.

2.6 Conclusions

In this chapter blanket wafers are used for the screening of both the physical and electrical properties of polycrystalline InAs, $In_xGa_{1-x}As$ and GaAs deposited by MBE, in view of their integration as channel materials in 3-D NAND memories.

Special attention is addressed to the mobility and the thermal stability. *Si*-doping, far below 1.5%, is realized during the III-Vs deposition, to conduct Hall mobility and Van der Pauw measurements. The thermal stability study is performed by applying ex-situ annealing in FGA ambient at temperatures ranging from 350 ˚C to 500 ˚C.

An attempt to create simple patterned structure is done with the aim to study the interface of III-V with oxides and the contact resistance when such compounds are contacted with metal. Unfortunately, the electrical characterization cannot be performed due to leakage current between the electrode most probably caused by the used fabrication route not suitable for polycrystalline layers.

GaAs does not emerge as a good candidate for the poly-Si channel replacement in 3-D NAND because of the difficulty encountered to contact such material. Indeed, the electrical characterization of GaAs layers is prevented by a too high contact resistance attributed to the Ga-As-O native oxides grown on the GaAs surface once the films are exposed to air. The oxidation of GaAs results in the formation of arsenic (*As*) excess near the interface and oxides such as Ga_2O_3 and As_2O_3 on the surface. Ga_2O_3 is one of the most stable Ga-oxides and it is difficult to be removed, representing a bottleneck for the integration and the electrical performance of GaAs [113]–[115].

Comparing $In_xGa_{1-x}As$ and InAs with similar carrier density n_s, the latter has superior conduction properties: higher μ and lower R_s, resulting from its intrinsic properties such as its lower band gap (0.36 eV).

$In_xGa_{1-x}As$ is slightly more robust against high temperature annealing as compared to InAs. This is suggested by the evolution of the grain size as a function of thermal treatments. InAs shows an increase in grain size with the anneal temperature, which in turn is beneficial in terms of μ, while no grain size variation is observed on $In_xGa_{1-x}As$ layers.

The morphological variations observed on InAs films upon thermal steps are expected to become worse when such material is integrated in constrained geometries such as our 3-D NAND.

Based on the obtained results, $In_xGa_{1-x}As$ shows a good compromise between mobility and thermal stability, resulting as a promising candidate to replace poly-Si as channel material in future 3-D NAND flash memories.

Chapter 3

Integration of epitaxially grown channel on single layer test vehicle

3.1 Introduction

This chapter focuses on two different aspects: the engineering of the grain (GS) in poly-Si channels and the integration of epitaxially grown Si and $Si_{1-x}Ge_x$ as replacement of poly-Si channel for 3-D NAND memories. The integration of epitaxially grown channels has the aim to assess the compatibility of the epitaxial process with our geometries in view of epi-III-V channels (Chapter 4). Both poly-Si and epitaxially grown channels are integrated in a 3-D test vehicle produced by imec. Such vehicle is designed to characterize the single vertical cell and mimics the gate-first/channel-last approach of the BiCS flow [54]. Poly-Si, which is the industrial relevant channel material, is used as reference.

As already discussed in (1.2.1), *Si* conduction depends on several factors such as the GS, defects at grain boundaries and within the grains. In order to investigate possible GS engineering and the impact of the GS on the channel conduction, different deposition conditions and thermal annealing are tested. The GS is then extracted by means of a visual estimation from STEM images and compared with the measured I_D for all the available channels.

Epi-Si is integrated as benchmark material against poly-Si channels. Beside pure epi-Si, epi-$Si_{1-x}Ge_x$, with a *Ge* content ([*Ge*]) of 25 at %, is also integrated as a stepping stone in view of the III-V integration. $Si_{1-x}Ge_x$, with

low [*Ge*], is chosen for its compatibility (e.g., in terms of thermal budget) with our poly-Si scheme; this means that it is possible to focus just on the challenges introduced by the replacement of poly-Si with a new channel material, without changing the other integration steps such as the junction formation. The most critical steps of the epitaxial process integration flow are monitored by SEM, FIB (Focused Ion Beam) and TEM inspections. The devices are then electrically characterized. The current conduction is studied by extracting the transconductance and results are interpreted through a resistive network model, to clarify the impact of channel defects on I_D. Finally, memory performance is also investigated in order to assess the impact of new channel materials on the ONO gate stack.

3.2 Poly-Si process flow

The Si-based process flow of "STRATO", imec's single-cell test vehicle is illustrated in Fig. 3.1.a. The process flow starts with an n+ implant into a 300 mm p-type *Si* wafer, to form the source junction. Then, 30 nm thick SiO_2, named bottom oxide (BOTOX), is deposited. The CG is formed on top of the BOTOX and it consists of 200 nm thick Low Pressure Chemical Vapor Deposition (LPCVD) *Si*, deposited at 710 ˚C. The CG is highly doped with boron (*B*) by ion implantation, followed by activation using a spike anneal at 1100 ˚C. Then, it is patterned and capped with 40 nm SiO_2, called top oxide (TOPOX), as shown in Fig. 3.1.b. After the memory hole lithography, vertical cylindrical memory holes with diameters ranging from 70 nm to 100 nm are etched through the TOPOX/CG/BOTOX layers. Next, the ONO memory stack is deposited in a reverse order (compared to planar Flash), starting from the memory hole sidewalls with a ~4.5 nm high temperature-deposited SiO_2 (HTO) BlOx, ~5 nm LPCVD Si_3N_4 charge trap layer and finally ~4 nm HTO TuOx, which is closest to the channel. To enable the connection of the channel to the source junction, the ONO stack is opened at the bottom of the memory hole, as shown in Fig. 3.1.c, using an anisotropic dry etching; since this step could damage the TuOx, a thin (~3 nm) sacrificial amorphous-Si (a-Si) protection layer is deposited on top of the TuOx immediately after the memory stack deposition. The a-Si also prevents TuOx attack during the diluted hydrogen fluoride (DHF) used to have a good interface between the source junction and the channel. Just after the DHF treatment, the memory hole is filled with LPCVD Si, which serves

both as channel and as drain. The drain thickness is ~180 nm. Different Si recipes are available, as summarized in Table 3.1: Si is deposited in the polycrystalline state, by using µC-Si and Std-Si recipes, or amorphous, and crystallized after either via Furnace Annealing at 650 ˚C (FA) or by Pulsed Laser Thermal Annealing (LTA), with a pulse duration < 200 ns.

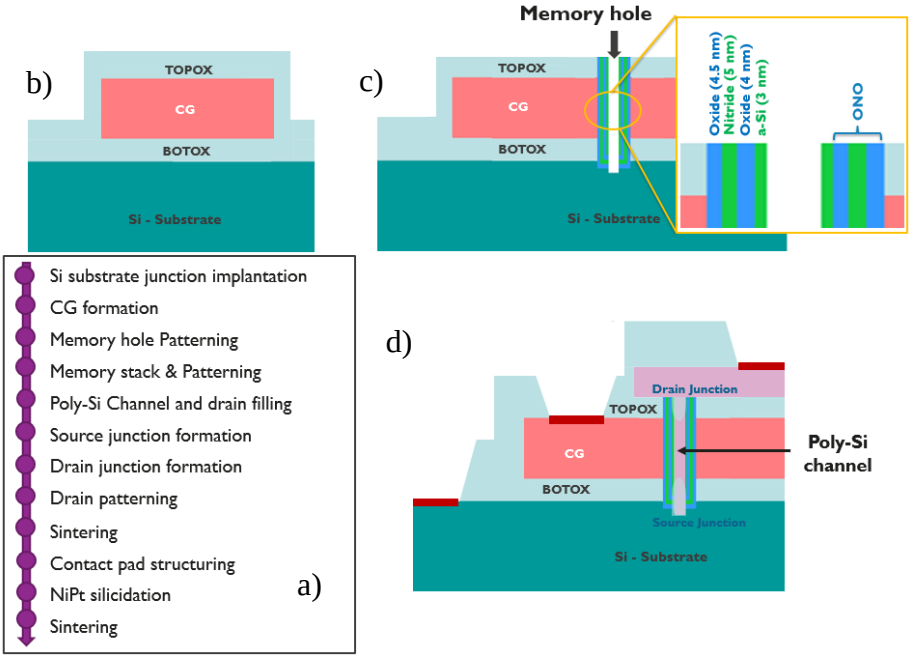


Figure 3.1: a) Poly-Si based process flow of our single cell 3-D NAND test vehicle. Schematic view of the test vehicle after b) CG formation, c) memory stack patterning, d) NiPt silicidation.

Recipe Name	Deposition temperature [°C]	Post deposition anneal
µC-Si	**710**	**--**
Std-Si	**720**	**--**
FA-Si	**600**	**650 °C/2h in FGA**
LTA-Si	**600**	**LTA (pulse duration < 200 ns)**

Table 3.1: Poly-Si channel recipes used in our single-cell test vehicle.

The source junction is formed by diffusion of *P* from the substrate to poly-Si during a 45 sec anneal at 1050 ˚C, while the drain junction is formed by an arsenic (*As*) implant, activated at 1000 ˚C for 1.5 sec. The final steps are: the contact pad formation, the Nickel-Platinum (NiPt) silicidation, applied to reduce the contact resistance, and passivation of the channel and its interface with the ONO, conducted in two steps using FGA. The first step is done after the drain patterning at 520 ˚C for 20 min, while the second sinter is done after the silicidation at 420 ˚C for 20 min. The completed test vehicle is shown in Fig. 3.1.d.

3.3 Process flow for epitaxially grown Si and $Si_{1-x}Ge_x$ channels

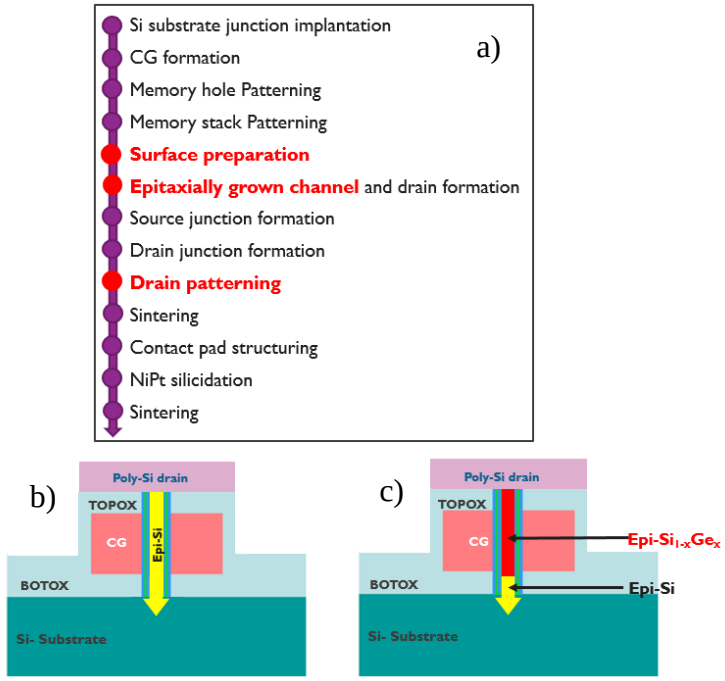


Figure 3.2: a) Epi-Si and Epi-$Si_{1-x}Ge_x$ process flow; added/modified steps with respect to poly-Si-based process flow are highlighted in bold red. Schematic view of the test vehicle after b) epi-Si channel and drain formation and c) epi-$Si_{1-x}Ge_x$ channel and drain formation.

The integration of epitaxially grown Si and $Si_{1-x}Ge_x$ as channel materials for our single layer 3-D NAND devices, requires an adaptation of the Si-based process flow. Figure 3.2.a highlights in red the modified steps for the integration of epi-Si and epi-$Si_{1-x}Ge_x$: surface preparation, channel growth, and drain pattering.

3.3.1 Surface preparation

Epitaxy is not just a deposition: it is a sensitive and selective process which allows the growth of a single crystalline film on top of a crystalline substrate [122]. One of the key parameters in order to have a good epitaxial growth is the nature of the surface, where the growth is initiated [122] and a proper surface preparation is required prior the growth. In our 3-D NAND structures the surface preparation is not straightforward, as it must also preserve the TuOx, to guarantee the memory performance.

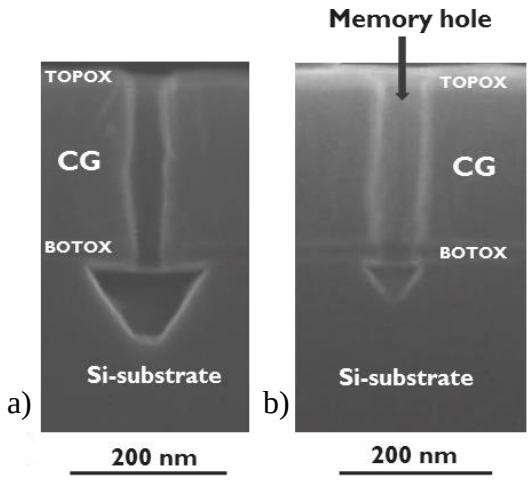


Figure 3.3: X-SEM inspections after a) 10 min treatment in pure chloridric acid (HCl) and b) 1 min of HCl. The conical shape in the Si-substrate is caused by the HCl etching chemistry. The latter treatment is used for the removal of the a-Si layer at the sidewalls.

The surface preparation starts with an ammonia-peroxide water mixture (APM) clean, which is applied for 5 min at 65 ˚C, to remove possible residues left after the memory stack opening. Thereafter, a DHF is used to remove the native oxide developed on the a-Si protection layer and on the Si substrate during vacuum break; such cleaning is also used in the poly-Si-based process flow. In addition, the sacrificial a-Si layer deposited to enable the source-bottom opening must be removed to prevent Si and $Si_{1-x}Ge_x$ growth at the sidewalls, which would lead to a premature closure of the memory hole. The a-Si removal is done by means of hydrogen chloride (HCl) vapor at 900 ˚C in a LPCVD system. The HCl etches the *Si* substrate below each memory hole along the (111) plane in a conical shape. This "void" represents the starting surface for the epitaxial growth and its depth can vary as a function of the exposure time of the substrate to HCl, as shown in Fig. 3.3: in the preliminary experiments, the HCl cleaning is applied for 10min, but it results in a too aggressive etch, with a void depth of ~100 nm (see Fig. 3.3.a). Therefore, the time is tuned from 10 min to 1 min, leading to a significant reduction of the conical shape (~40 nm of depth) as shown in Fig. 3.3.b.

3.3.2 Channel and drain formation

Epi-channels are grown just after the HCl cleaning step in the same LPCVD system.

Epi-Si is grown from the substrate to the top surface at a growth temperature of 810 ˚C. Then, 180 nm thick poly-Si is deposited at 650 ˚C, in-situ, on top of the channel, to form the drain, as shown in Fig. 3.2.b.

For the case of epi-$Si_{1-x}Ge_x$, the integration is conducted in three in-situ subsequent steps (Fig. 3.2.c), to keep unaltered the formation of the drain and source junction with respect to the Si-based scheme. First, 50 nm of epi-Si is grown at the bottom of the memory holes using the conditions reported above, to keep unmodified the source junction. Next, the epi-growth is switched to $Si_{1-x}Ge_x$, at a temperature of 700 ˚C, and with a nominal [Ge] equal to 25 at %, to create the channel. Finally, the drain is deposited identical to the epi-Si case.

Figure 3.4 shows the FIB inspection conducted after the deposition of the epi-Si source/epi-$Si_{1-x}Ge_x$ channel/poly-Si drain structure: the epi-Si growth is well tuned and stops just in line with the top part of the BOTOX (Fig. 3.4.a). On the other hand, the epi-$Si_{1-x}Ge_x$ growth is difficult to

control. The epi $Si_{1-x}Ge_x$ channel does not always stop at the memory hole mouth, but sometimes an overgrowth is observed, as shown in Fig. 3.4.a (first memory hole on the left). As a consequence, the poly-Si drain deposition, which should be ~180 nm thick, results in rough poly-Si surface (Fig. 3.4.a), since it is mixed locally with the overgrowth of epi-$Si_{1-x}Ge_x$, as illustrated in Fig. 3.4.b.

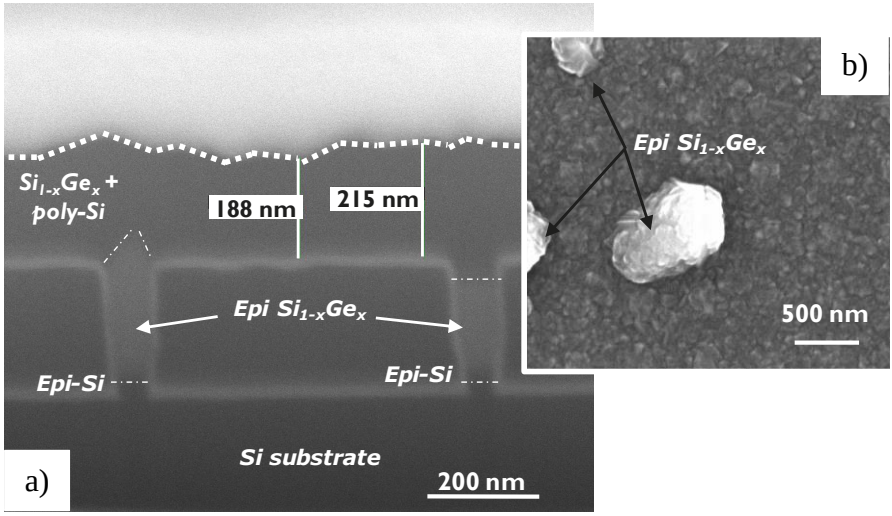


Figure 3.4: a) FIB inspection after the deposition of the epi-Si source/epi $Si_{1-x}Ge_x$ channel/poly-Si drain structure in three in-situ

3.3.3 Junctions formation and drain patterning

The formation of source and drain junctions are unaltered with respect to the one in poly-Si based integration flow. However, for the $Si_{1-x}Ge_x$ devices, the conventional drain patterning recipe has to be tuned, to ensure proper etch of the poly-Si drain, which is mixed locally with $Si_{1-x}Ge_x$ channel overgrowth.

The drain patterning consists of a lithographic step followed by an etching: ~400 nm of PR is first deposited on top of the drain. The surface is then exposed to light in order to transfer the pattern which is present on the used mask. Afterwards, the part of exposed drain is etched and an in-situ strip is used to remove the PR left on the un-exposed drain. The strip is

based on carbon tetrafluoride (CF_4) and oxygen (O_2) and it is followed by 2 sec dip in 1.5 % aqueous HF.

Figure 3.5.a shows the FIB inspections conducted after the tuned drain etch followed by the strip: the drain comes out as patterned properly, without attacking the TOPOX and the CG underneath, but ~ 150nm of PR is still on top of the drain, meaning that the strip treatment is not able to remove it totally. A possible explanation can be that during the patterning some by-products of the reaction are deposited on the PR, working like a mask for the strip. During the HF cleaning (which follows the strip), all the residues are removed. To ensure that the PR is totally removed (Fig. 3.5.b), a second strip, identical to the first one, is required and has been applied.

Finally, the rest of the process flow (e.g., contact formations, silicidation, FGA treatment) follows unmodified.

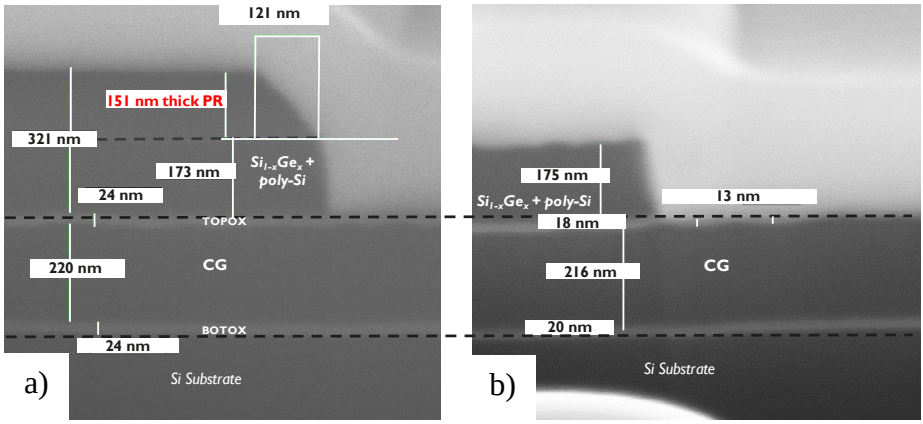


Figure 3.5: a) FIB inspection after drain patterning plus in-situ strip for the PR removal. The existing in-situ strip is not efficient, and only part of the PR is removed. b) FIB inspection after extra ex-situ strip. The PR is completely removed from the drain.

3.4 TEM analysis

To assess the quality of epitaxially grown channels, and the interface with the TuOx, STEM inspections are conducted. For this purpose, two different types of STEM are used: High-Angle Annular Dark Field

(HAADF)-STEM and DF-STEM. The HAADF-STEM contrast is proportional to the thickness of the TEM specimen and to $<Z>^2$, where Z is the atomic number, and it is used to analyze the thicknesses of the ONO layers. The DF-STEM contrast is related to the density and crystallinity (such as grains, defects) of the different layers and it is used to study the quality of the channels.

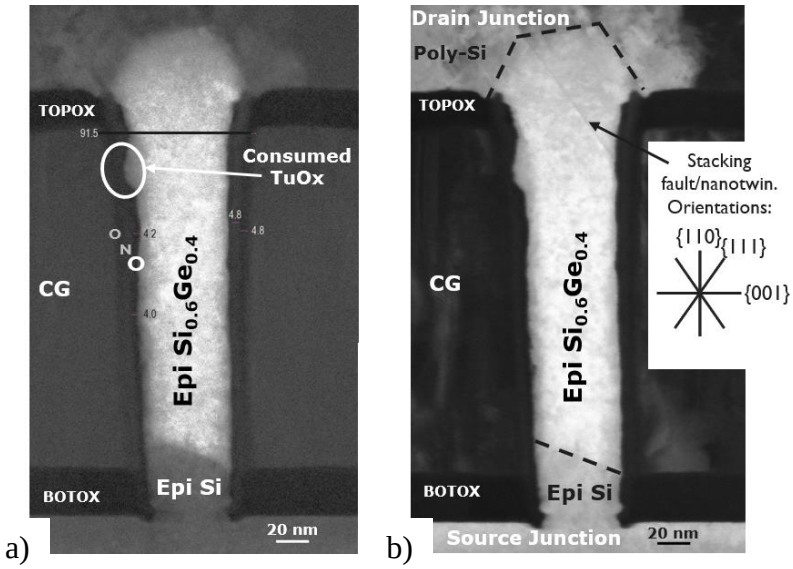


Figure 3.6: a) HAADF-STEM and b) DF-STEM for epi-$Si_{1-x}Ge_x$ channel with a diameter of ~60 nm. The TuOx is not continues at the sidewalls. The channel is overgrown and it is characterized by some planar defects.

Figure 3.6 shows the STEM pictures of epi-$Si_{1-x}Ge_x$ devices: the TuOx is not continue along the memory holes and in some areas (highlighted with a circle in Fig. 3.6.a) it is totally consumed. The channel, as already discussed, is overgrown and is characterized by the presence of some stacking faults/nanotwins in the {111} planes. Stacking faults and nanotwins are planar defects and can be described as an interruption of the regular atomic sequence in a local region of the crystalline material [123]. Furthermore, Energy Dispersive X-Ray Spectroscopy (EDS) (not shown) is conducted doing STEM measurements to extract the [*Ge*]: on average the [*Ge*] is ~40 at %, showing a significant shift from the initial nominal value of 25 at %.

Similar to the case of epi-$Si_{1-x}Ge_x$, epi-Si devices also present a consumed and non-uniform TuOx, as shown in Fig. 3.7.a. The thickness of the TuOx is ~ 1-1.5nm thinner than the expected value. Thinner TuOx compromises the memory performance of our devices, as will be reported in (3.8). An in-depth investigation to understand the origin of the TuOx consumption will be conducted in Chapter 4. The DF-STEM of epi-Si channel is shown in Fig. 3.7.b: the channel presents many planar defects along {111} planes.

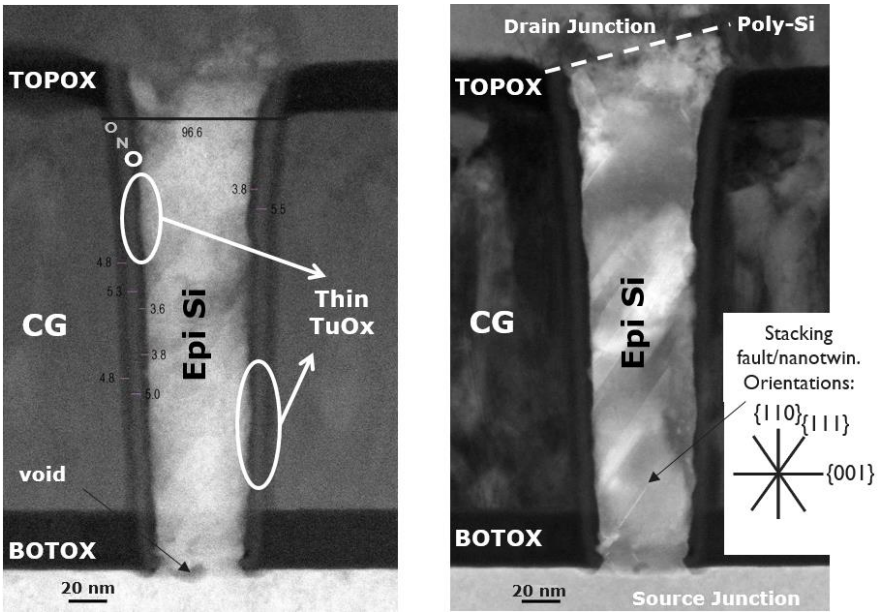


Figure 3.7: a) HAADF-STEM and b) DF-STEM for epi-Si channel with a diameter of ~60 nm. The TuOx is thinner than the expectation and it is not continues at the sidewalls. The channel has planar defects.

3.5 Evaluation of the grain size impact on poly-Si channels

The GSs of the poly-Si channels integrated by using several recipes (see Table 3.1) are computed through imaging tools and reported as D_{EQ}, as described in (2.3.2). Given the small dimension of the channel diameter

(~50 nm), DF-STEM measurements on a specimens of thickness of ~30 nm are used instead of TD-SEM analysis, to assess the crystallinity of the channels and extract the GS. DF-STEM images offer just a cross sectional view of the channel. Therefore, they allow only a 2-D analysis of the GS.

Only the grains in focus, and hence clearly observable and within the plug area considered, as shown in Fig. 3.8: in the middle of the channel the grains are more clear than those at the interface and it emerges that the LTA-Si channel has the largest GS (Fig. 3.8). This result is more evident by analyzing the distribution of the D_{EQ}, reported in Fig. 3.9: µC-Si and Std-Si show a similar result. FA induces larger grains as compared to µC-Si and Std-Si, while the largest grains are obtained with the LTA recipe.

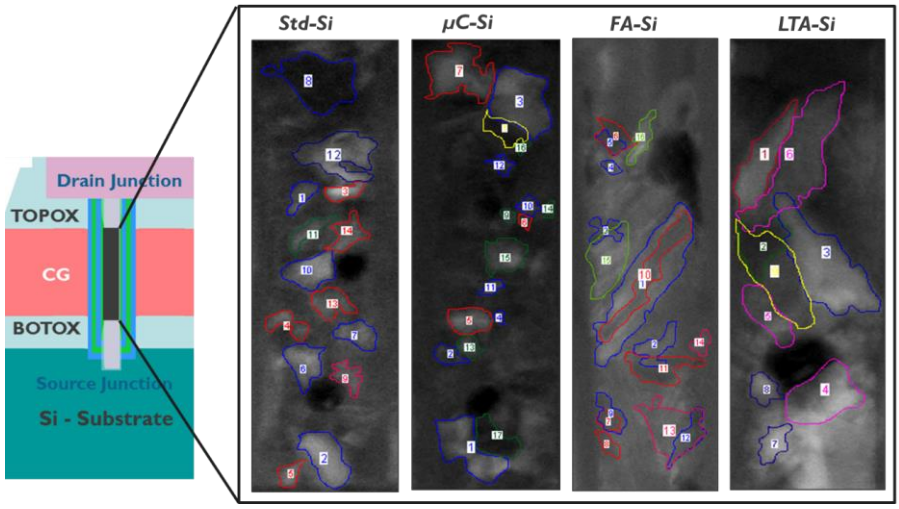


Figure 3.8: processed DF-STEM pictures of poly-Si channels grown using different recipes (Tab. 3.1). Each marked area represent a different grain into the channel.

The impact of the GS enlargement on the I_D is shown in Fig. 3.10: it is found that the I_D in 3-D NAND memories can be boosted by engineering the poly-Si channel GS, through LTA rather than FA. However, the I_D improvement is not only caused by the GS increase. Indeed it has been demonstrated that LTA also results in a better channel-oxide interface and less defective grain boundaries [76], [82], both beneficial for the channel conduction. Epi-Si is added in Fig. 3.10 as benchmark channel material: as grain boundaries are absent, the epi-Si conduction is of course the best. The

properties of epi-Si channel will be discussed in more detail in the following sections.

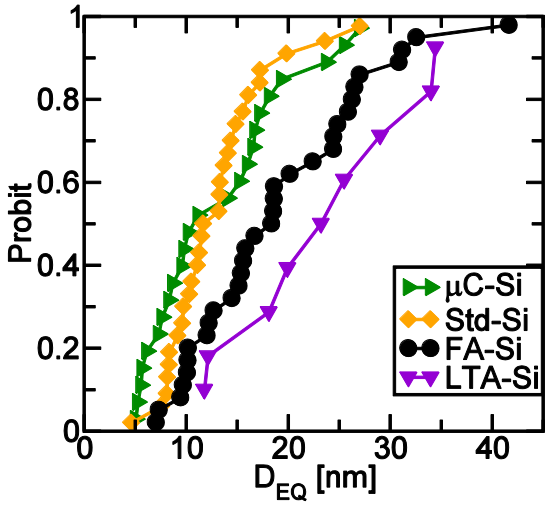


Figure 3.9: Distributions of the D_{EQ} extracted by analyzing from 1 up to 3 different DF-STEM images for all the available poly-Si channel recipes (Table 3.1). LTA-Si has the largest grains.

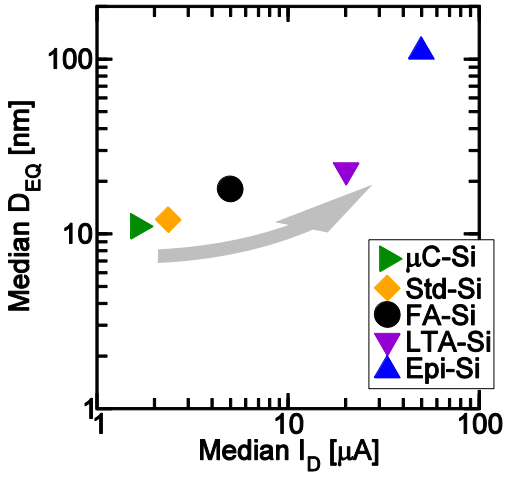


Figure 3.10: Median value of I_D as a function of the median value of the extracted D_{EQ}, for all the available Si channel. Epi-Si channel is added as benchmark material and shows the best conduction properties.

3.6 Electrical characterization

In the used maskset there are two typologies of electrical devices, namely dense and isolated. The dense devices consist of an active memory hole, with a narrow drain, surrounded by dummies, which are not electrically active, as shown in Fig. 3.11.a. On the other hand, the isolated devices are not surrounded by other structures and they have a larger drain, as shown in Fig. 3.11.b.

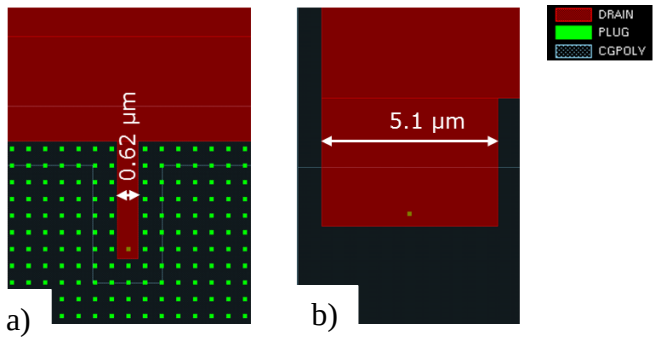


Figure 3.11: Schematic view of a) dense and b) isolated cells. Memory holes are shown in green, while the drain line is in brown.

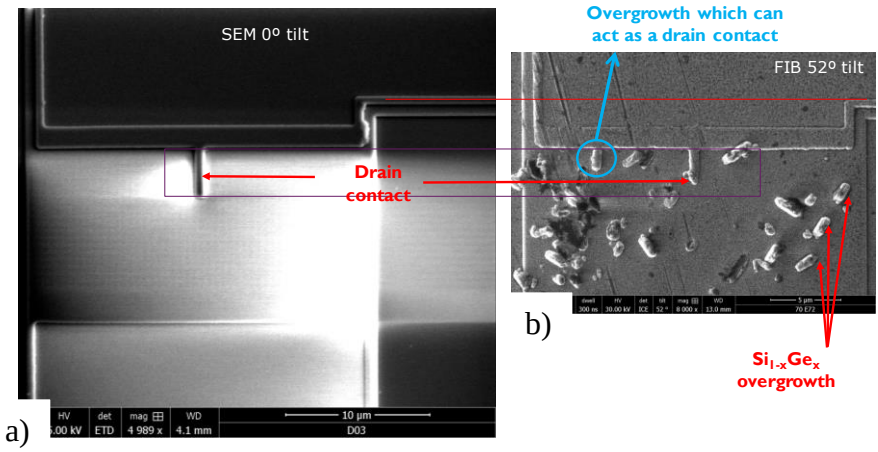


Figure 3.12: SEM and FIB images of poly-Si drain line on a dense structure respectively for a) poly-Si and b) epi-$Si_{1-x}Ge_x$ devices; overgrown $Si_{1-x}Ge_x$ can act as drain, shorting many holes.

In the case of $Si_{1-x}Ge_x$ channels, the dense structures cannot be used for the electrical characterization due to the $Si_{1-x}Ge_x$ overgrowth from the memory holes. Figure 3.12.a shows a SEM picture of a typical poly-Si drain line on devices with poly-Si channels: the surface around the active hole is clean and the drain contact has the expected length. Totally different results are instead observed on epi-$Si_{1-x}Ge_x$ devices, as illustrated in Fig. 3.12.b: the drain patterning over the plug is not properly done and the drain fin seems too short to reach the memory hole of interest. However, the overgrowth of $Si_{1-x}Ge_x$ such as the one highlighted with the blue circle in Fig. 3.12.b, can behave as drain, contacting more than one plug.

To ensure that only one device is measured, the electrical characterization is conducted exclusively on isolated holes. The equipment used for the I_D-V_G measurements is an Agilent B1500A semiconductor parameter analyzer. The Source Measure Units (SMUs) are used to apply 1V to the drain and a constant ramp to the gate.

Figure 3.13 compares the typical I_D-V_G characteristics for FA-Si, epi-Si and epi-$Si_{1-x}Ge_x$, showing the large improvement of epi-Si over the other channels. This can be better observed by plotting the statistical distribution of the I_D at V_{ov} equal to 2 V, as shown in Fig. 3.14: the median value of I_D in epi-Si is ~10 times higher than the one in poly-Si channels. Epi-$Si_{1-x}Ge_x$ performs slightly better than poly-Si, thanks to the absence of grain boundaries, but has worse conduction compared to epi-Si. To better understand this result, the μ values of perfect single crystal $Si_{1-x}Ge_x$ are shown in Fig. 3.15 as a function of the [*Ge*] [116]: the graph has the shape of a valley. The mobility decreases as the *Ge* content x increases up to 0.2 and remains constant up to 0.8; the latter value represents the turning point at which μ starts to increase, raising above the epi-Si μ for x higher than 0.95. According to the graph of Fig. 3.15, $Si_{0.6}Ge_{0.4}$ (which corresponds to the composition measured in our devices) has a much lower μ as compared to epi-Si one (~250 cm^2/Vs against ~1400 cm^2/Vs). As a consequence the I_D will be lower as well, in agreement with our results. However, Fig. 3.15 represents only a reference to understand how the conduction can change as a function of [*Ge*], but this does not mean that the reported μ values correspond to the ones of our epitaxially grown 3-D NAND channels. Indeed, in our case the μ is expected to be lower, due to the presence of defects into the channel (stacking faults and nanotwins) and at the interface.

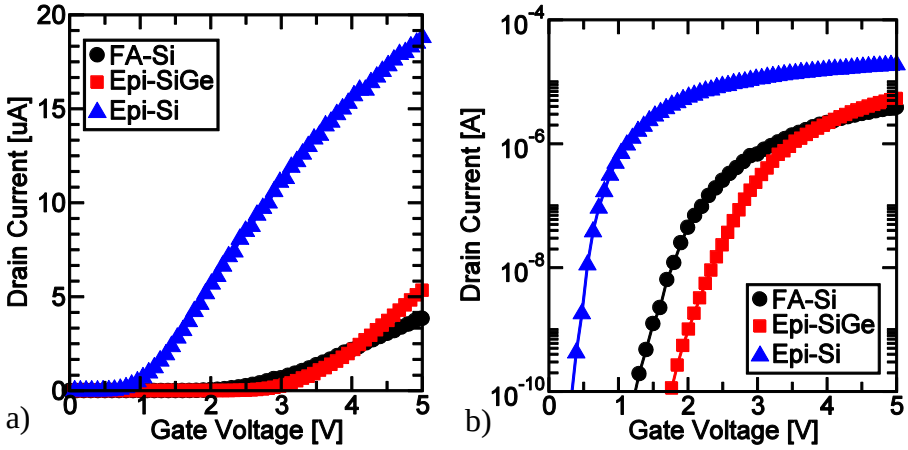


Figure 3.13: Typical I_D-V_G in a) linear scale, and b) logarithmic scale. The electrical characterization is performed on channel with a diameter of ~50 nm, by sweeping the gate up to 5 V while keeping 1 V at the drain.

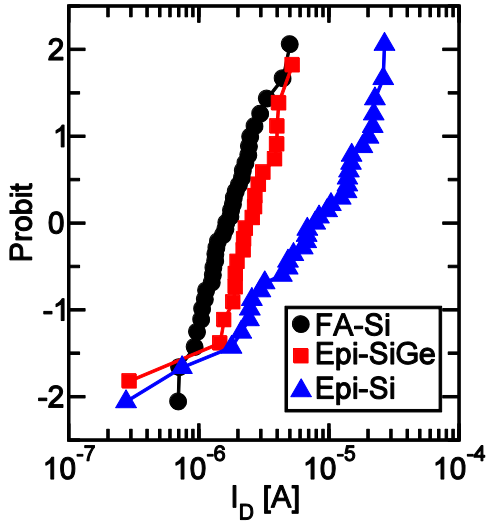


Figure 3.14: Statistical distribution of I_D at fixed overdrive voltage ($V_{ov} = V_{GS} - V_{th}$) equal to 2 V for FA-Si, epi-$Si_{1-x}Ge_x$, and epi-Si channels. Epi-Si shows the highest current.

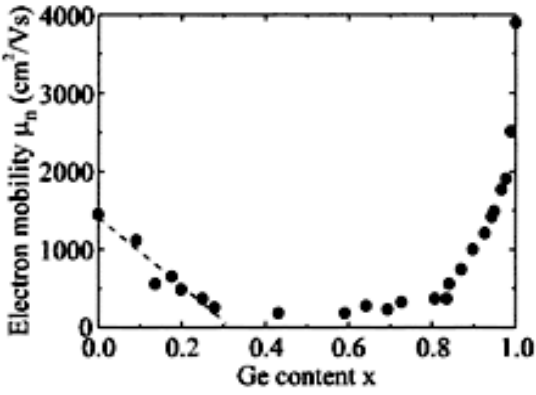


Figure 3.15: Electron mobility of perfect single crystal $Si_{1-x}Ge_x$ as a function of [*Ge*]. [116] The μ decreases as the *Ge* content x increases up to 0.2 and remains constant up to 0.8, value for which the mobility starts to increase, overcoming the epi-Si one for x higher than 0.95.

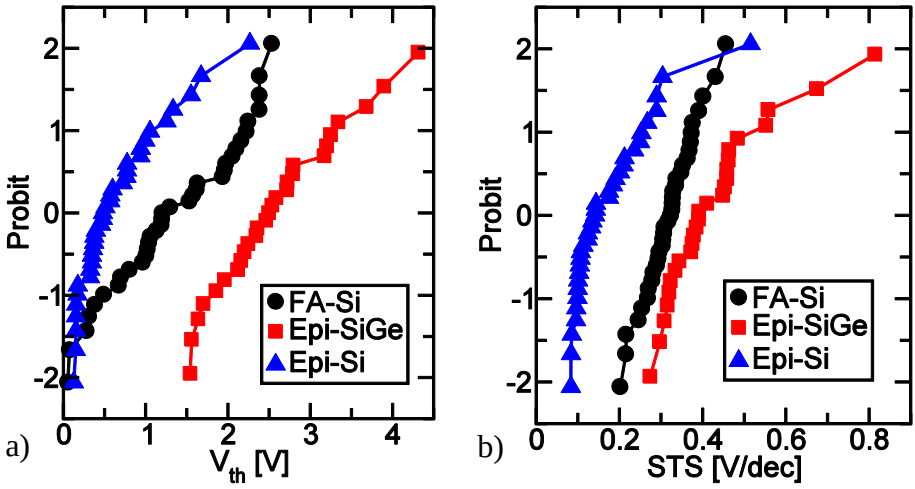


Figure 3.16: Distributions of a) V_{th} recorded at a target current of 30 nA, and b) Sub-threshold swing (*STS*). Epi-Si has the best *STS* with a bimodal behavior and the lowest V_{th}.

A clear improvement of epi-Si over the other channels is also observed in V_{th} and *STS* distributions reported in Fig. 3.16.a and Fig. 3.16.b, respectively. In epi-Si channels, the values of V_{th} are close to 0 V, while the

STS distribution appears to be bimodal: a tightly distributed mode is centered around 70 mV/dec and a more widely distributed mode is observed, with *STS* values that stretch up to ~300 mV/dec. Epi-$Si_{1-x}Ge_x$ shows instead the highest *STS* and V_{th}. This is a clear indication of the presence of a high trap density at the $Si_{1-x}Ge_x$/TuOx interface. Indeed, a higher interface trap density will delay the formation of the inversion layer, resulting in high *STS* and V_{th}.

Figure 3.17 shows the I_D at fixed V_{ov} equal to 2 V, as a function of the *STS*, from where a direct correlation can be found between these parameters: devices with better conduction also show a better behavior in *STS*. FA-Si and epi-Si are in the same trend line, while epi-$Si_{1-x}Ge_x$ results are slightly different, showing better I_D for similar *STS* compared with FA-Si.

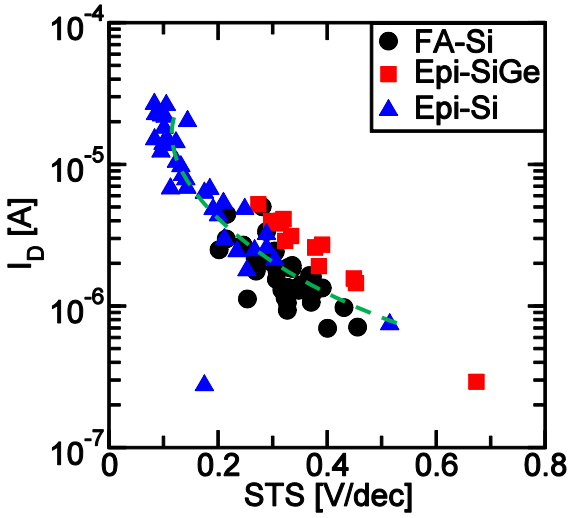


Figure 3.17: I_D at fixed V_{ov} equal to 2 V as a function of the *STS* for poly-Si, epi-$Si_{1-x}Ge_x$ and epi-Si channels. Devices with better *STS* show improved I_D.

The conduction properties of our channels are studied through the analysis of the tranconductance (g_m). The measurements for the g_m extraction are performed with a high voltage resolution (1 mV/step) and a fast sampling time (20 ms). Keithley 2602A SMUs are used to apply 100 mV to the drain and a constant ramp voltage to the gate.

By performing high resolution I_D-V_G in poly-Si channels, individual defect charging events can be distinguished. In poly-Si channels the conductions proceed through limited number of percolation paths between the source and the drain [5], [124], as shown in Fig. 3.18.a. If during the conduction a single electron is captured by a trap located near the percolation path, a I_D drop is observed, with a consequent ΔV_{th} (Fig. 3.18.b). Since the total ΔV_{th} increases with the gate voltage, the I_D-V_G curve is stretched out. Therefore, a proper analysis of the conduction properties of our channels can be done only if the charging component is separated. To filter out the charging component, the g_m is extracted around a fixed voltage called V_{sense}, as the slope of the I_D-V_G in linear regime and in between the charging events (Fig. 5.18.b). More details about the extraction of the g_m can be found in [5], [124].

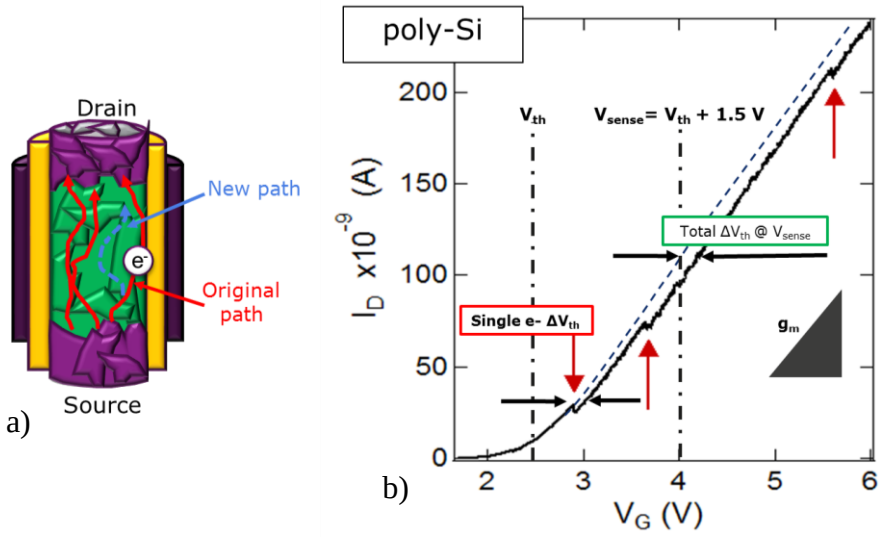


Figure 3.18: a) Percolation paths in a poly-Si channel; the current path is partially blocked if a trap close to it captures an electron. b) Discrete drops of I_D due to the trapping of electrons along the conduction path; 'Single e- ΔV_{th}' is the shift of the V_{th} caused by a single electron, while 'Total ΔV_{th}' represents the shift of the V_{th} at a fixed voltage called V_{sense}. V_{sense} is fixed to V_{th} + 1.5 V and is the voltage around which the g_m is extracted [5].

Ideally, in a single crystal channel the conduction should happen only along one conduction path (single grain), but in reality the planar defects into the channel and defects at interface cause charging events. Therefore, the procedure explained above for the extraction of the g_m in poly-Si can be also be applied to epi-Si and epi-$Si_{1-x}Ge_x$ channels.

Figure 3.19 shows the statistical distributions of charge-free g_m: epi-Si exhibits the best g_m, which is bimodally distributed. In the next section it will be demonstrated that the low-g_m mode in epi-Si is due to the stacking faults, while the high-g_m mode corresponds to the single-grain behavior.

The g_m distribution of epi-$Si_{1-x}Ge_x$ devices is at the level of mode-1 in epi-Si and is three times higher than the poly-Si one (Fig. 3.19).

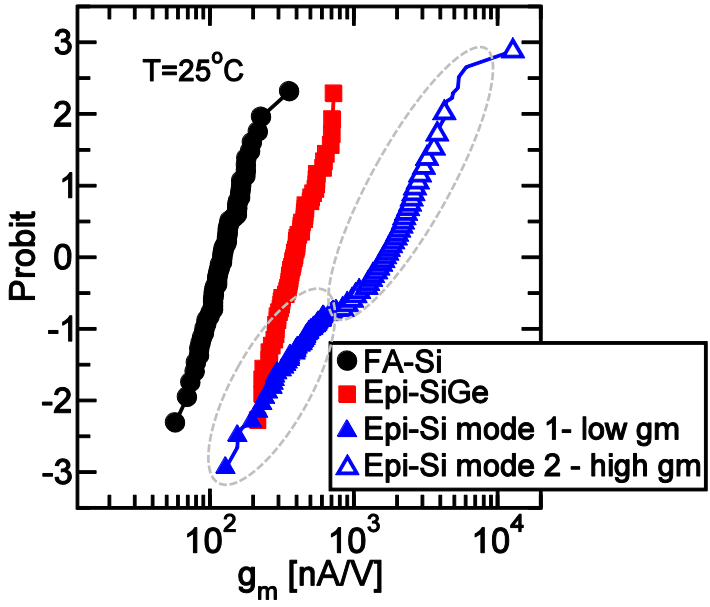


Figure 3.19: Statistical distribution of g_m for poly-Si, epi-$Si_{1-x}Ge_x$ and epi-Si devices. Epi-Si g_m is bimodal corresponding to either defects-controlled g_m (mode 1) or single-grain-controlled g_m (mode 2).

3.7 In-depth electrical characterization: statistical analysis of g_m

In this section a resistive network model, developed to simulate the statistical behaviour of the g_m in scaled poly-Si channel devices [6], is applied to provide a thorough understanding of the bimodal behaviour in g_m observed for the epi-Si channel in Fig. 3.19. In summary, the current flow between source and drain is modeled by using a 2-D resistive network, with the assumption that the conduction is dominant on the cylindrical surface of our channels. The cylindrical channel is first un-wrapped and then the grains and a grid of resistors are projected on top of it, as shown in Fig. 3.20. The choice of the grid size determines the resolution of the simulation. The number of grains in the channel (N_{grains}) is a user defined parameter, while a Monte-Carlo algorithm generates Si grains from randomly positioned nucleation centers (Fig. 3.20).

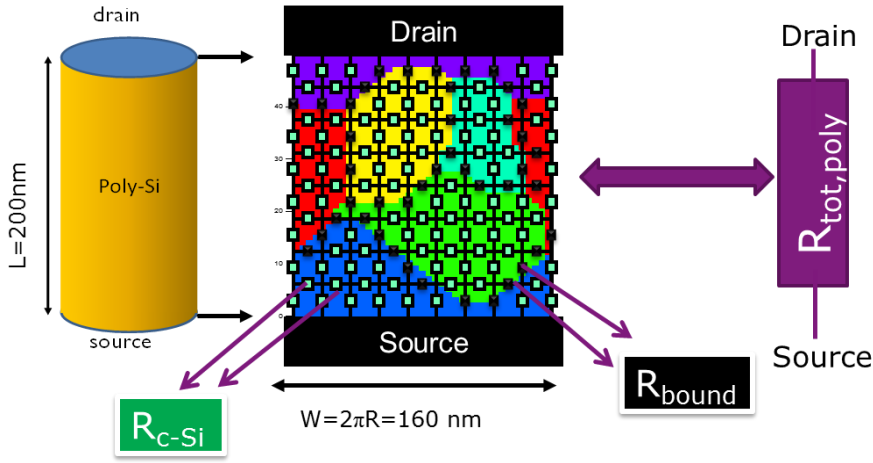


Figure 3.20: the surface conduction of cylindrical Si channels is modeled as a resistive network [6]. Each grain into the resistive network is represented with a different color.

The value of the resistors inside a crystal grain ($R_{c\text{-}Si}$), is increased by a factor γ for resistors at the grain boundaries (R_{bound}), according to Eq. 3.1[6]:

$$R_{bound} = \gamma R_{c-Si} \tag{3.1}$$

The value of $R_{c\text{-}Si}$ is in turn defined by the Eq. (3.2) [6]:

$$R_{c-Si} = \frac{V_{DS}}{g_{m,c-Si}\alpha ln\left(1+exp\left(\frac{V_G-V_{th}}{\alpha}\right)\right)} \frac{n_x}{n_y-1} \quad , \tag{3.2}$$

where α is the parameter which describes the transition from the sub-threshold to the linear regime, n_x and n_y represent the nodes of the network; typically, simulations are conducted by considering a network with $n_x \cdot n_y$ equal to 47·60. $g_{m,c\text{-}Si}$ is the modelled g_m into the grains, which is calculated using data from single crystal Si FinFETs, as described in detail in [6].

By applying the resistive model, it was already shown that the variance of the g_m measured on a large number of identical devices increases when the average number of grains in the channel decreases [6]. For a perfect epitaxially grown channel, a distribution without any variance would be expected, since no grain boundary-induced variability exists.

In order to explain the bimodality observed in our epi-Si channels, simulations are conducted starting from one grain and increasing the N_{grains} progressively. Simulations are carried out by keeping the parameter γ constant and no variations from any source other than the geometric distribution of grains is assumed.

Figure 3.21 shows the simulated g_m distributions for channels with N_{grains} increasing from 1 up to 8: for a 1-grain configuration, a single value corresponding to the maximum possible g_m is found. As the number of grains increases, bimodal and multimodal distributions are generated; for 8 grains, the multiple modes can no longer be distinguished and an apparent single-mode distribution with wide spread is obtained. The origin of the multiple modes is traced back to the number and the spatial configuration of the grains in the device. As an example, in Fig. 3.22 the devices with exactly 2 grains give rise to a bimodal distribution. The extremes correspond to a completely blocking grain boundary (mode-1, lowest gm) and a perfectly source-to-drain aligned grain boundary (mode-2, maximum g_m possible value).

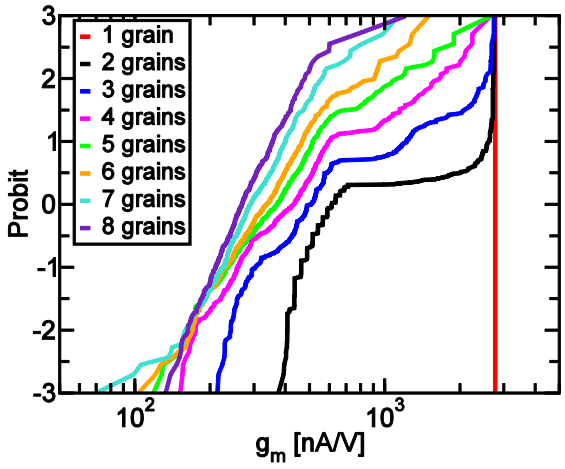


Figure 3.21: Simulated g_m distributions considering different numbers of grains (N_{grains}); as the N_{grains} increases, bimodal and multimodal distributions are generated [125]. The single grain g_m value is taken from FinFET data [6].

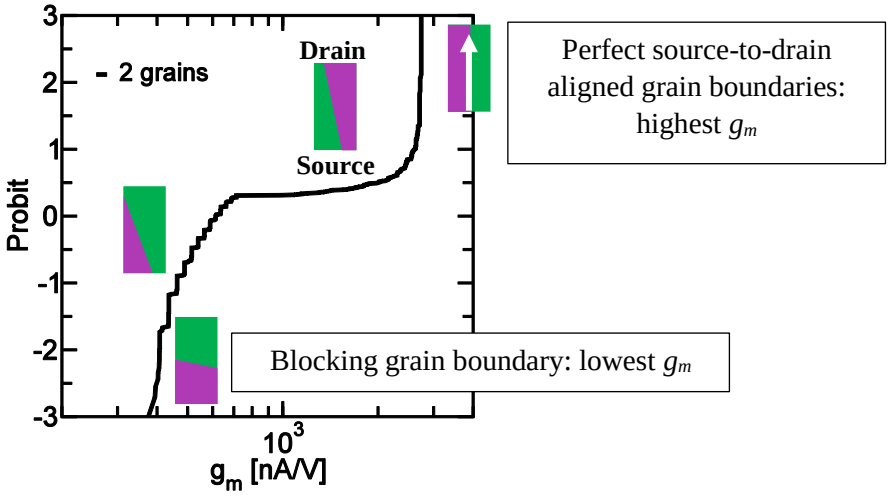


Figure 3.22: Simulated g_m distribution using exactly 2 grains. The modal behaviour is related to the possible grain configurations (schematically illustrated with the green/purple rectangles) [125].

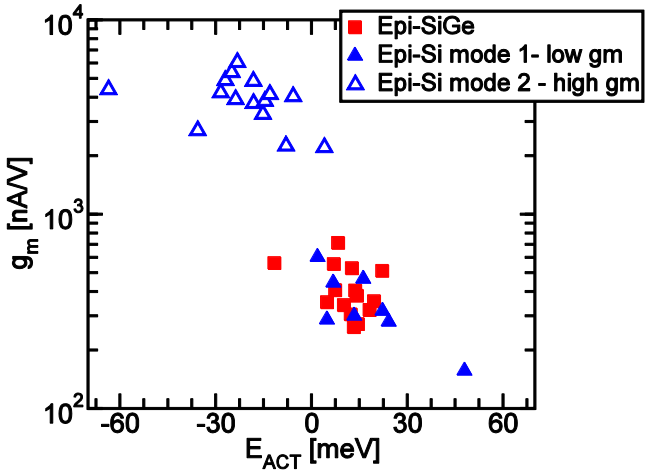


Figure 3.23: Correlation between g_m and E_{ACT} for epi-$Si_{0.6}Ge_{0.4}$ and epi-Si. Epi-Si is characterized by two population of devices. Devices with high g_m show a negative E_{ACT}, while devices with low g_m have a positive E_{ACT}, as for the case of epi $Si_{1-x}Ge_x$.

When attempting to fit the measured bimodal g_m distribution on epi-Si (Fig. 3.19) with the bimodal distribution of Fig. 3.22, an additional spread on the maximum g_m value has to be added, which should originate from multiple other sources of variability such as geometric device-to-device variations (channel length, width, dielectric thickness, etc..). However, after this modification, a good fitting of the epi-Si data is still not achieved (not shown): a simulation with exactly 2 grains does not quantitatively reproduce the measured g_m distribution.

To fit the measured g_m, the mechanisms which are causing the bimodality have to be first understood. For this purpose, the activation energy (E_{ACT}) of both epitaxially grown channels is extracted by using an Arrhenius dependence through Eq. 3.3:

$$E_{ACT} = \frac{ln\frac{g_{m,T_1}}{g_{m,T_2}}}{\left(\frac{1}{kT_2}-\frac{1}{kT_1}\right)} \quad , \tag{3.3}$$

with T_1 = 298K and T_2 = 398K.

Figure 3.23 shows that epi-Si g_m for mode-1 devices increases with temperature (positive $E_{ACT} \approx 15$ meV). This behavior is typically associated with thermionic emission over grain boundaries in polycrystalline materials [126]. The epi-Si g_m for mode-2 devices on the contrary, decreases with temperature (negative $E_{ACT} \approx -20$ meV). Such phenomenon is caused by scattering-controlled single crystal mobility [126]. Therefore, it can be concluded that mode-1 at low g_m (comprising 34% of the measured devices) is grain boundary-limited, while mode-2 at high g_m (comprising the 66% of the measured devices) reflects the single-crystal value without any grain boundary obstruction.

For epi-$Si_{1-x}Ge_x$ devices, the g_m temperature dependence coincides with that of mode-1 in epi-Si, as shown in Fig. 3.23. This means that the conduction in all the measured epi-$Si_{1-x}Ge_x$ channels is controlled by thermionic emission over a barrier. This barrier can come from the defects at the interface with the gate stack, or at the interfaces between the channel and the Si junctions, given the different lattice constant for both materials [116].

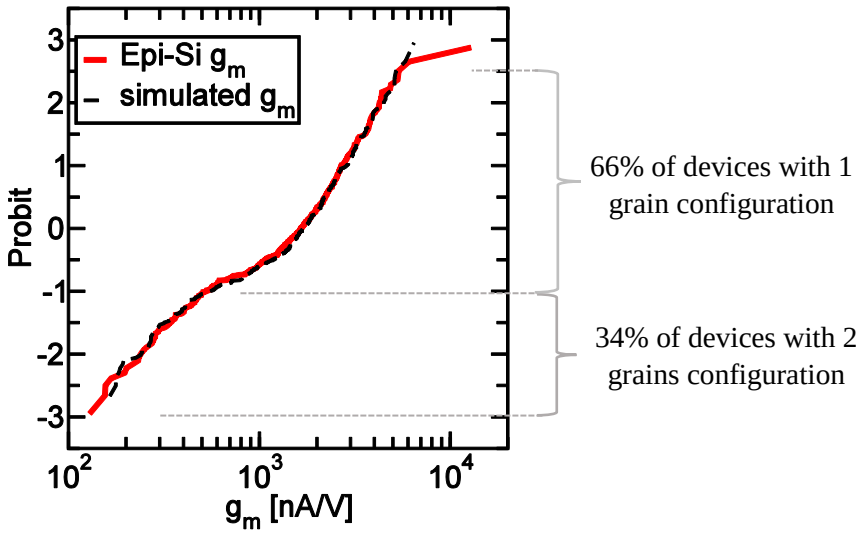


Figure 3.24: Correlation between observed epi-Si g_m data and simulated g_m with distributed N_{grains} (66% single grain and 34% 2 grains configuration) [125].

Based on the results of Fig. 3.23, an excellent g_m fitting can be finally obtained by assuming 66% of the devices having 1 grain and 34% having 2

grains (Fig. 3.24). The used γ-value is equal to 160 and it is significantly lower than the values reported in poly-Si ($\gamma \approx 700$) [6]. This indicates that in epi-Si, the possible grain boundaries are less 'resistive' and could be interpreted as stacking faults or nanotwins rather than poly-Si-like grain boundaries, as also concluded from TEM inspections (Fig. 3.7).

3.8 Memory performance

Figure 3.25 shows ISPP and ISPE of epitaxially grown and FA-Si channels. Programming is conducted using 100 µs program pulses, while the erase is performed by applying 1 ms erase pulses. *P/E* curves are performed from the fresh state and they are reported as the medians of the ΔV_{th} relative to the fresh state acquired on ~10 devices. Both epi $Si_{1-x}Ge_x$ and epi-Si show faster ISPP/ISPE at low voltages than FA-Si. *P/E* characteristics are sensitive to the TuOx thickness. Therefore, the obtained results are a clear signature of a thinner TuOx, as already observed in STEM inspections (Fig. 3.6 and Fig. 3.7). Furthermore, the consumption of the TuOx is also corroborated by long-term retention test conducted on epi-Si channels.

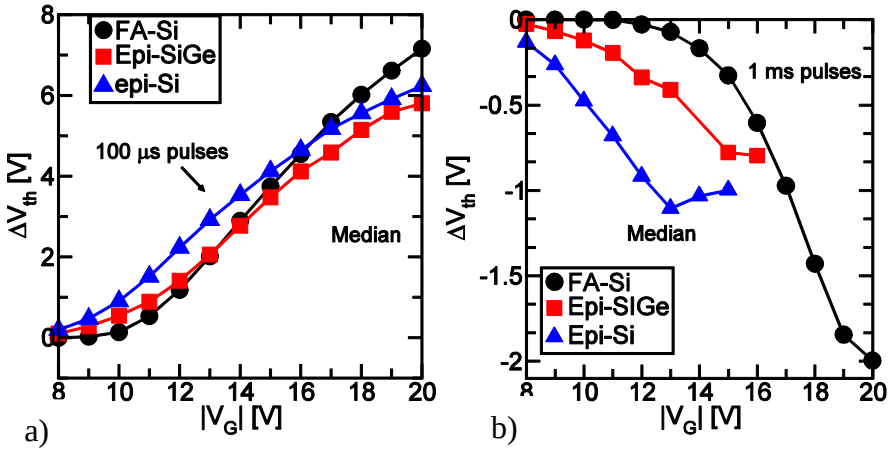


Figure 3.25: a) ISPP with 100-μs program time and b) ISPE with 1 ms erase time, for different types of channels with a dimeter of ~60 nm. Epitaxially grown channels show faster ISPP and ISPE.

Retention measurements are performed at room temperature and reported in Fig. 3.26: ~10 devices are programmed to achieve ΔV_{th} = 4 V from their fresh state, and then the V_{th} is monitored for ~1 week. Epi-Si shows a retention loss of ~0.6 V already after 1 hour.

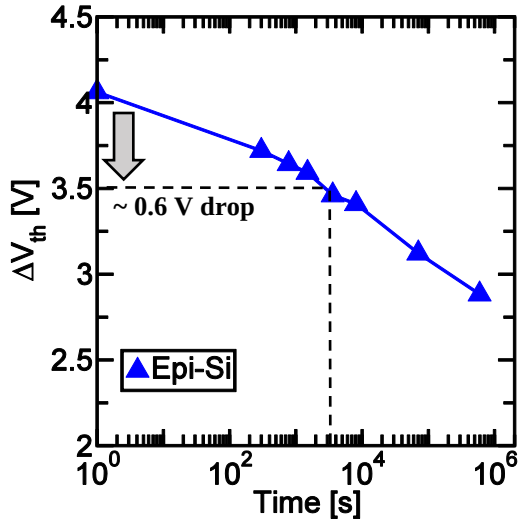


Figure 3.26: Long-term retention for epi-Si channels with a diameter of ~60 nm. Epi-Si shows a voltage drop of ~0.6 V already after 1 hour.

3.9 Conclusions

Impact of GS on poly-Si channel conduction

The GS of different flavors of poly-Si channels is extracted via a visual estimation from STEM images. It is observed that the GS enlargement can be achieved by crystallizing as-deposited a-Si through LTA rather than FA. The engineering of the channel grain size (GS), in turn, can boost the conduction properties of the channel. However, the observed I_D enhancement is not only attributed to the GS increase, but also to the reduction of defects at interface and at grain boundaries [76].

Integration of epitaxially grown channels

Epi-$Si_{1-x}Ge_x$ and epi-Si are used as a stepping stone toward the III-V channel integration in 3-D NAND memories, with the aim to investigate the

challenges introduces when poly-Si channel is replaced with an alternative material. The poly-Si-based process flow is modified to cope with the integration requirements of the epitaxially grown material. The integration scheme requires a careful preparation of the starting *Si* surface to allow a growth exclusively from the bottom opening of the memory hole; this is achieved by properly cleaning native oxides and by removing the a-Si from the memory hole sidewall.
From the integration of epitaxially grown channels three important aspects emerge:

a) The TuOx is partially consumed, compromising the memory performance. This phenomenon can be caused by the surface preparation required prior to the epitaxial growth of the channel.
b) Epi-$Si_{1-x}Ge_x$ is always accompanied by an overgrowth which is mixed locally with poly-Si drain. As a consequence, the poly-Si drain is not uniform and a tuning of the drain etch is required to have a proper drain formation.
c) A significant drift of the nominal [*Ge*] is observed when the $Si_{1-x}Ge_x$ recipe, developed for planar structures is transferred in constrained geometries, such as our 3-D NAND channels. The measured [*Ge*] is ~40 at % as compared to the nominal value of 25 at %.

Electrical characterization

In this study epi-Si and epi-$Si_{1-x}Ge_x$ channels are benchmarked against poly-Si, to investigate the impact of the grain boundaries on current conduction. The epi-Si channel shows the best conduction properties, with large improvements on both *STS* and g_m over epi-$Si_{1-x}Ge_x$ and poly-Si channels.

The experimentally observed g_m bimodal distribution for epi-Si is explained through a resistive network model: lower g_m conduction occurs when the current needs to cross a higher resistance boundary associated with planar defects into the channel. On the other hand, devices with higher g_m indicate the absence of defects in the channel. The conduction in epi-$Si_{1-x}Ge_x$ also shows improvements over poly-Si. However the analysis of the current has shown that the conduction is controlled by defects, which may be positioned at interface with the TuOx, or at the Si source and drain junctions, given the difference in lattice mismatch.

Chapter 4

III-V channel integration on three layer test vehicle

4.1 Introduction

This chapter focuses on the most challenging steps to integrate epitaxially grown $In_xGa_{1-x}As$ as replacement of poly-Si channel for 3-D NAND and on the impact this will have on the electrical performance.

$In_xGa_{1-x}As$ is integrated on "SAKKARA", imec's 3 gates vertical test vehicle, that uses poly-Si as reference channel material; the side gates, named top select gate (TSG) and bottom select gate (BSG), are used as selectors, while the central gate represents the memory cell, as described in sections (4.2) and (4.3). The 3 gates test vehicle is more relevant and realistic than the single cell test vehicle introduced in Chapter 3. It follows the same integration sequences of a BiCS-based flow [54]: the gate patterning is done after the memory hole formation, contrary to the approach used in the single layer test vehicle. Furthermore, as it mimics a string, it allows to study the effects of the spaces between the gates and to control the junctions by means of the selectors.

Regarding the III-V process integration, special attention is given to three different aspects:

a) **Surface preparation** required to initiate the III-V growth: HCl and chlorine (Cl_2) routes are investigated and their impact is studied through physical and electrical characterization.

b) **III-V epitaxial growth**. The channel filling capability and its composition are assessed by exploring different *Ga* precursors, flow ratios and growth temperatures.

c) **Drain and contact formation**, which has to comply with the low thermal budget of III-V channels.

The conduction properties of $In_xGa_{1-x}As$ channels are finally analyzed by considering different In composition, x, ranging between 0.25 and 0.55, and are compared with those of the Si-reference.

4.2 Poly-Si process flow

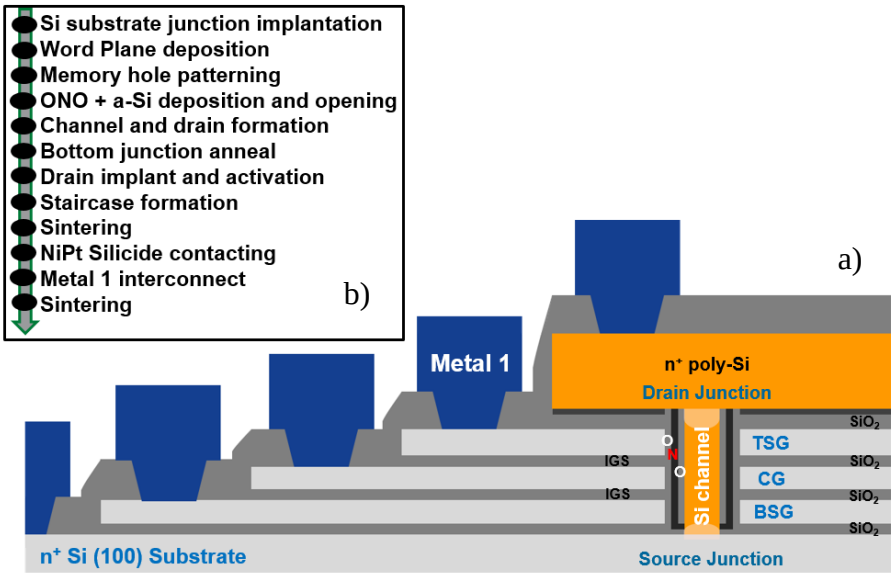


Figure 4.1: a) Outline of the production process of our 3 cells 3-D NAND test vehicle with poly-Si channel. b) Poly-Si-based process flow.

The Si-based process flow of our three-layer test vehicle is outlined in Fig. 4.1.a, while the schematic view is shown in Fig. 4.1.b. It starts with the implantation of P, and its activation at 1050 ˚C for 120 sec, into a 300 mm p-type Si wafer, to form the source junction. Then, the word planes stack is deposited: it consists of three layers, implying 50 nm a-Si deposited by

LPCVD and highly doped with B, and interleaved by a 30 nm thick SiO_2 Inter Gate Spacing (IGS) layer. A spike anneal at 1100 ˚C is used both to activate the gate dopants and to crystallize the a-Si layers.
Vertical cylindrical memory holes with diameters ranging from 70 to 100 nm are etched through the entire stack. Then, the ONO memory stack, consisting of ~5.5 nm BlOx, ~4.5 nm Si_3N_4 trapping layer and ~4 nm TuOx, is deposited by LPCVD. The connection of the channel with the substrate source junction follows the same procedure as used in our single layer test vehicle (3.2): a thin a-Si layer is deposited on top of the TuOx immediately after the memory stack deposition as protection and a dry etch is applied to open the ONO at the bottom of the memory hole. Next, the memory holes are filled by LPCVD a-Si, used also to form the drain junction on top. The Si crystallization is then induced either via FA or by LTA (3.2). The junctions are kept unchanged with respect to the ones in the single layer test (3.2): *P* is diffused from the substrate to poly-Si channel at 1050 ˚C for 45 sec, to form the source junction, while *As* is implanted and then activated at 1000 ˚C for 1.5 sec, to form the drain junction. Once the junctions are created, a staircase is fabricated to allow to contact the drain, the TSG, the CG and the BSG; the patterning of each single layer requires a lithographic step followed by etching. The contact formation starts with the deposition of CVD SiO_2 at 480 ˚C, to isolate the various layers. Afterwards, the oxide is opened, a NiPt silicidation is done on the contact openings to reduce the contact resistance and vias are created by depositing and patterning the Metal 1; this consists of 30 nm of TiN and 500 nm of *Al*, which is Copper-doped to reduce the *Al* electro-migration [127]. The two sintering steps, also used in the single layer test vehicle (3.2) to improve the current performance, are applied before the NiPt silicidation and after the Metal 1 formation.

4.3 Integration of the $In_xGa_{1-x}As$ channel: process flow

The replacement of poly-Si channel with an alternative material requires an adaptation of the Si-based process flow, similarly to what has been already done for epi-$Si_{1-x}Ge_x$ in Chapter 3. Fig. 4.2.a highlights in red the main modified steps for the integration of epitaxially grown $In_xGa_{1-x}As$ channel, namely surface preparation, channel growth, drain and staircase

formation. As already observed in Chapter 3, the surface preparation required to enable a proper channel formation is a critical step, as it must preserve the ONO memory stack. The surface preparation etches the Si substrate preferably along the {111} plane in a conical shape, which will represent the starting surface for the III-V growth (Fig. 4.2.a). To grow the channel properly, an appropriate tuning of precursors, in combination with growth temperature and flow ratio is also needed.
Moreover, thermal processes which require temperatures higher than 650 ˚C might cause degradation as well as inter-diffusion of $In_xGa_{1-x}As$. Therefore, to cope with the lower III-V thermal budget, the formation of source and drain junctions has to be modified with respect to the Si-reference flow, which has a thermal budget as high as 1050 ˚C.

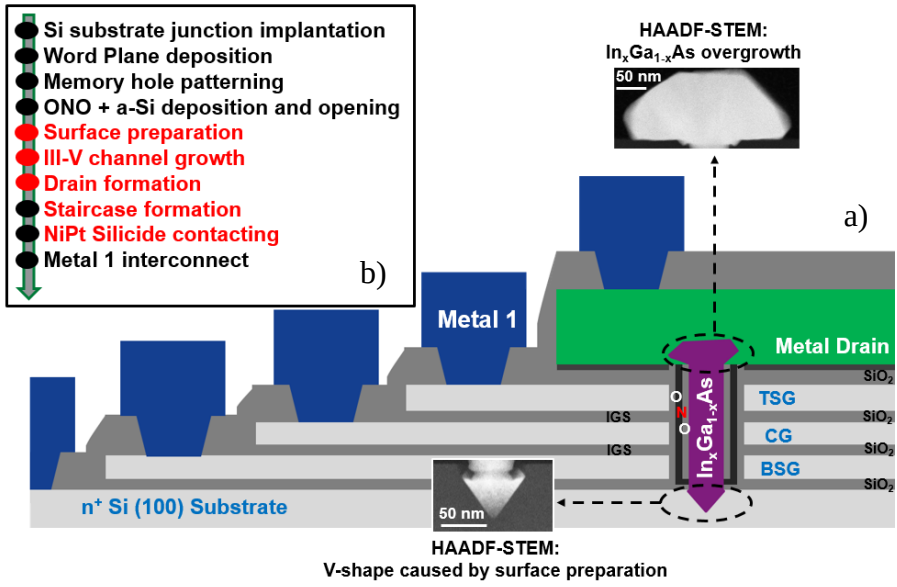


Figure 4.2: a) Schematic view of our 3 cells 3-D NAND test vehicle with $In_xGa_{1-x}As$ channel. b) Production process of $In_xGa_{1-x}As$ device; added/modified steps with respect to poly-Si-based process flow are highlighted in red.

4.3.1 Surface preparation

The main purpose of the surface preparation in our flow is to remove the native SiO_2 formed during the vacuum break between the memory hole opening and the III-V deposition. Furthermore, the a-Si layer remaining at the sidewalls after the source-bottom opening must be removed to prevent III-V growth at the sidewalls, which would lead to a premature closure of the memory hole (3.3.1). Two surface preparation routes are used, namely based on HCl and Cl_2.

The HCl route uses DHF to remove the Si native oxide developed on the a-Si and on the *Si* substrate, as already seen in (3.3.1). Afterwards, the exposed a-Si is removed in a reduced pressure chamber by using HCl vapor.

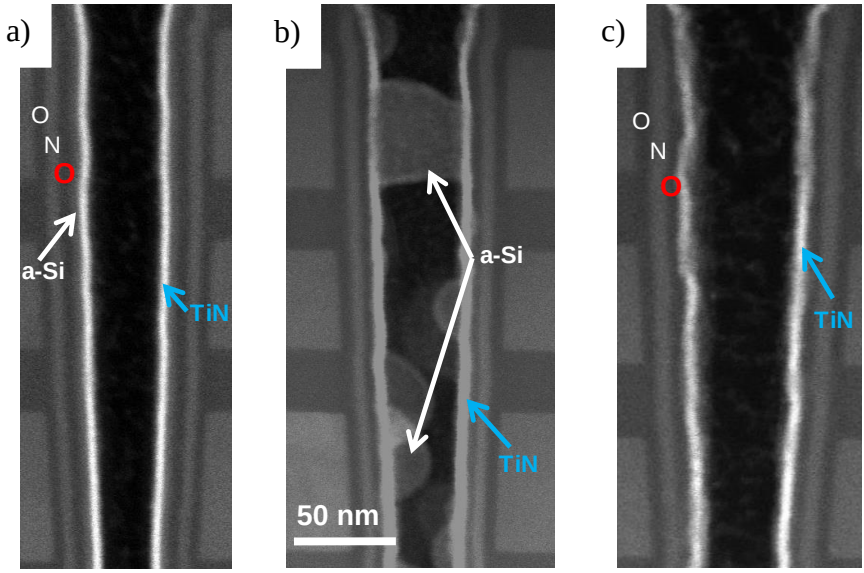


Figure 4.3: HAADF-STEM of individual trenches after a) HF-dip to remove native oxides, b) bake at 900 ˚C as thermalizing step and c) bake plus HCl to remove the a-Si. After the bake a displacement of the a-Si layer is observed. After the complete cleaning the TuOx, marked with the red O is not uniform. Titanium nitride (TiN) is deposited as decoration layer to get a better contrast of the ONO stack.

To characterize the impact of the HCl on the integrity of the memory stack, HAADF-STEM observations have been conducted before and after the treatment in HCl. The assessment of the ONO stack is difficult to do in our cylindrical memory holes, due to the interference created by the curvature effect. Therefore, trench-like structures with a length of 2 µm are used instead of the memory holes, to obtain a better contrast of the ONO. Figure 4.3.a shows a HAADF-STEM inspection conducted after the HF step: the TuOx appears continuous on the sidewalls thanks to the a-Si protection layer. On the contrary, Fig. 4.3.c shows that after the HCl treatment, the TuOx is not uniform. The HCl cleaning is composed of two steps: bake, used as thermalizing step, plus HCl, both made at 900 ˚C in H_2 ambient. At such high temperature, *Si* migrates on the surface [128]–[130], as shown in Fig. 4.3.b. The *Si* displacement leaves the TuOx exposed, which consequently will be reduced by the H-atmosphere [128]–[130] upon HCl exposure. Since the HCl and the III-V growth are executed in two different tools, an in-situ remote plasma assisted dry etch, called SiCoNi^{TM} [131] is added just before the III-V deposition to remove the native oxide developed on the Si substrate. This cleaning process consists of three steps: active species based on fluoride components (e.g., ammonium fluoride (NH_4F)) are generated in a plasma chamber by combining nitrogen trifluoride (NF_3) and ammonia (NH_3). Then, the chemical etching of the native oxide is given by the reaction between NH_4F and SiO_2 at room temperature; this reaction creates solid by-products, which are sublimated afterwards by using a bake below 200 ˚C. The SiCoNi^{TM} is applied on multiple cycles. The amount of removed SiO_2 depends on both the duration of the reaction between NH_4F and SiO_2 and on the numbers of cycles for which the SiCoNi^{TM} is applied. In the structures under investigation the TuOx is already exposed and it might be further consumed by SiCoNi^{TM}. Figure 4.4.a shows a X-SEM inspection after 6 cycles SiCoNi^{TM} treatment followed by the III-V growth: ~25 nm of top oxide of the word plane is removed and a III-V growth, most probably starting from the upper part of the TSG, closes prematurely the memory hole. Therefore, the number of SiCoNi^{TM} cycles is reduced from 6 to 1, to preserve the thickness of the top SiO_2 (as well as that of the TuOx), allowing a proper III-V growth from the Si substrate, as shown in Fig. 4.4.b.
To compensate for the consumption caused by the HCl route, the TuOx is thickened by ~1.5 nm.

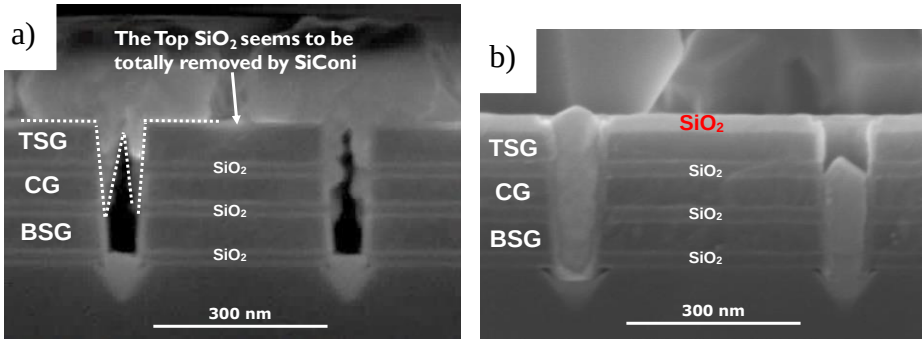


Figure 4.4: X-SEM inspection after III-V growth. a) Premature closure of the memory holes and consumption of the top oxide are observed due to 6 cycles SiCoNi^{TM} treatment. b) Memory holes are properly filled and the top oxide is on target after the reduction of the number SiCoNi^{TM} cycles.

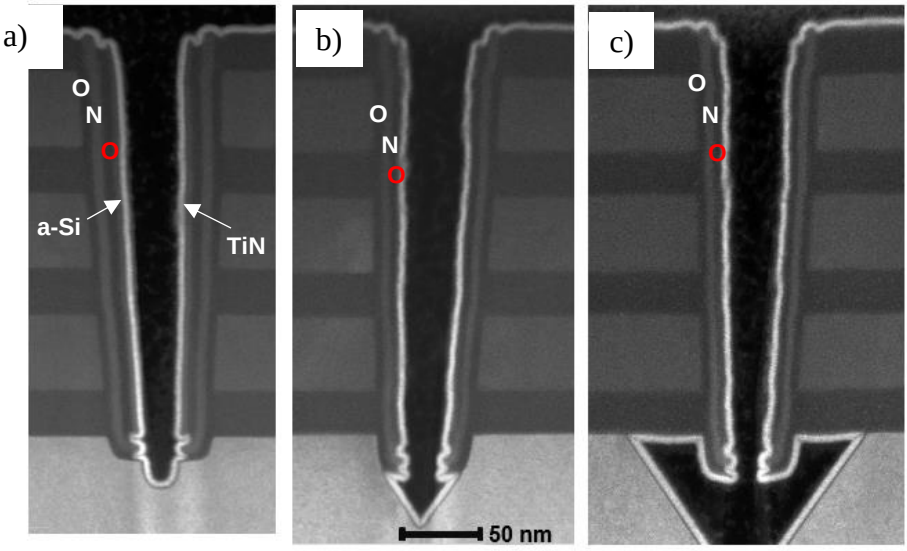


Figure 4.5: HAADF-STEM of individual trenches after HCl cleaning at a) 650 ˚C, b) 750 ˚C, c) 800 ˚C. TiN is deposited as decoration layer. The a-Si layer is removed only starting from 750 ˚C.

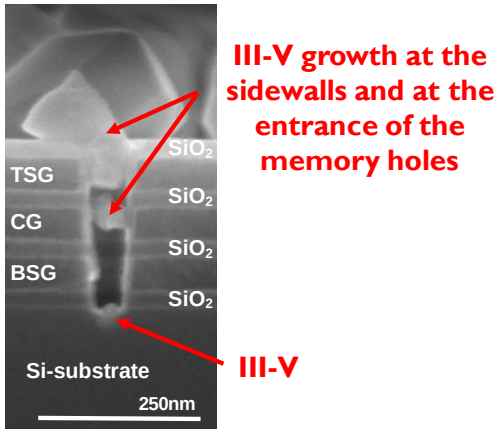


Figure 4.6: X-SEM inspection after III-V growth. III-V grows at the mouth of the memory hole and at the sidewalls, due to the presence of a-Si not totally removed during 30 min of HCl at 750 ˚C.

The HCl is also tested at lower temperatures and for 30min, as shown in Fig. 4.5: at 650 ˚C the HCl is not able to remove the a-Si layer at the sidewall. The HCl seems to become effective starting from 750 ˚C (Fig. 4.5.b): the a-Si is not present at the sidewalls, the TuOx profile appears continuous and the substrate is etched in a conical shape whose dimension increases with the temperature (e.g., 800 ˚C, as shown in Fig. 4.5.c). Unfortunately, such results are not always reproducible and during the III-V channel formation a premature closure of the memory holes is observed in some experiments (Fig. 4.6) due to the presence of a-Si at the sidewalls.

Alternatively to the HCl, a Cl_2 route for the a-Si removal is proposed. Contrary to the HCl route, this cleaning consists of two in-situ successive steps: first, SiCoNi^{TM} is used as native SiO_2 removal without attacking the TuOx, since it is still protected by a-Si. Then, Cl_2 at 600 ˚C in N_2 ambient replaces HCl in H-atmosphere just prior to III-V growth. The Cl_2 route is preferred to the first route as it dissociates efficiently at lower temperatures than HCl [132], [133]; this may help to prevent severe TuOx reduction and further consumption. To compensate for some possible consumption, ~ 0.5nm thicker TuOx is deposited. Figure 4.7 compares the ONO stack after HCl and Cl_2 routes: contrary to what happens with HCl cleaning (Fig. 4.7.a), the TuOx stays uniform after the Cl_2 route (Fig. 4.7.b).

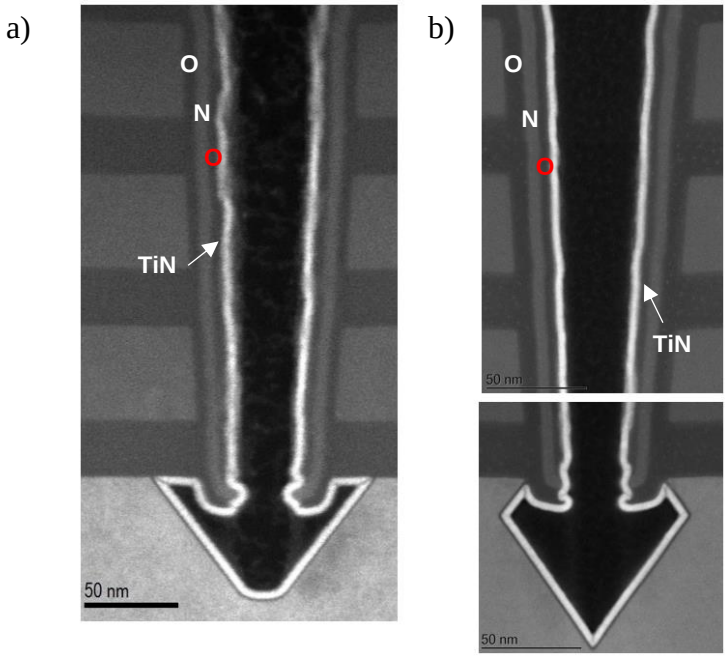


Figure 4.7: HAADF-STEM of individual trenches after a) HCl route and b) after Cl_2 route. TiN is deposited as decoration layer to have better contrast of the ONO stack. The TuOx stays uniform after the Cl_2 cleaning.

Table 4.1 summarizes the thicknesses of FA-Si and $In_{0.45}Ga_{0.55}As$ channels with the two different cleaning routes.

Recipe Name	**Cleaning route**	**TuOx thickness [nm]**
FA-Si	DHF (a-Si is not removed)	~4
H45	HCl	~4 + ~1.5
C45	Cl_2	~4 + ~0.5

Table 4.1: TuOx thicknesses of poly-Si (FA-Si) and $In_{0.45}Ga_{0.55}As$ channels with two different cleaning routes.

4.3.2 Channel formation

After the surface preparation, the channel is epitaxially grown by a CVD method, known as MOVPE, or also MOCVD [134], [135]. The name of this technique (metal organic vapor phase epitaxy), is originated by the fact that it uses metal-organic molecules as precursors, as shown in Fig. 4.8.a. The conventionally used molecules for $In_xGa_{1-x}As$ growth are: Trimethylindium (TMIn), Trimethylgallium (TMGa), and Tertiarybutylarsine (TBAs). However triethylgallium (TEGa) can be seen as an interesting option to replace TMGa, as it decomposes at lower growth temperature (T_{growth}), with the advantage to reduce the Carbon (*C*) incorporation [136], [137]. In III-V materials *C* acts as a dopant [138].
At room temperature all the precursors are liquid, and they are stored in containers called bubblers (Fig. 4.8.a). Since each precursor is stored in a different bubbler, the $In_xGa_{1-x}As$ composition can be adjusted by tuning the precursor transport into the chamber. H_2 is used as carrier gas to transport the precursor into the reactor. H_2 is introduced in the bubblers (Fig. 4.8.a) and it bubbles through the metalorganic liquid, which reacts partially in a vapor phase and starts to diffuse to the heated substrate surface into the chamber. When these molecules flow over the hot substrate, a series of surface reactions occur, as shown in Fig. 4.8.b; they starts to decompose, due to the impact with the heated surface. The pure elements are incorporated into the substrate, contributing to the $In_xGa_{1-x}As$ growth, while the methyl, ethyl and butyl groups react with H_2, desorb and are pumped away. In order to have a growth with the proper selectivity (e.g., growth only on Si and not on oxide areas), it is also important to find the proper combination of the growth conditions (e.g., flow ratios, T_{growth}, etc..).
It is quite common to grow at low pressure such as 20 Torr, but it is also possible to go up to 750 Torr [91]. The growth rate depends on the precursors transport into the chamber but also on other parameters such as the fact to grow on patterned or blanket wafers. However, one of the most important key parameters is to choose the right T_{growth} to allow an efficient decomposition of the precursors and to make sure that *C* is not incorporated in the III-V material.

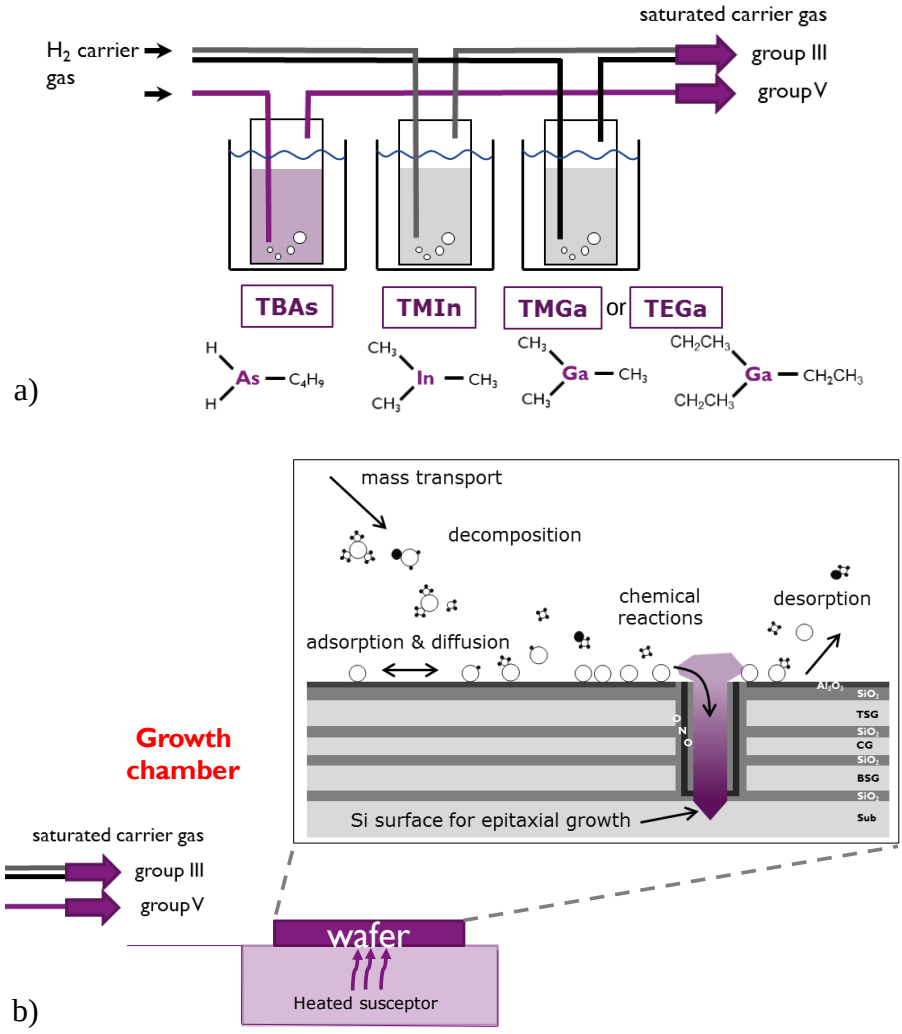


Figure 4.8: a) Metal-organic precursors and carrier gas used for the $In_xGa_{1-x}As$ growth by MOVPE technique. b) Sketch of the surface reactions involved during the MOVPE.

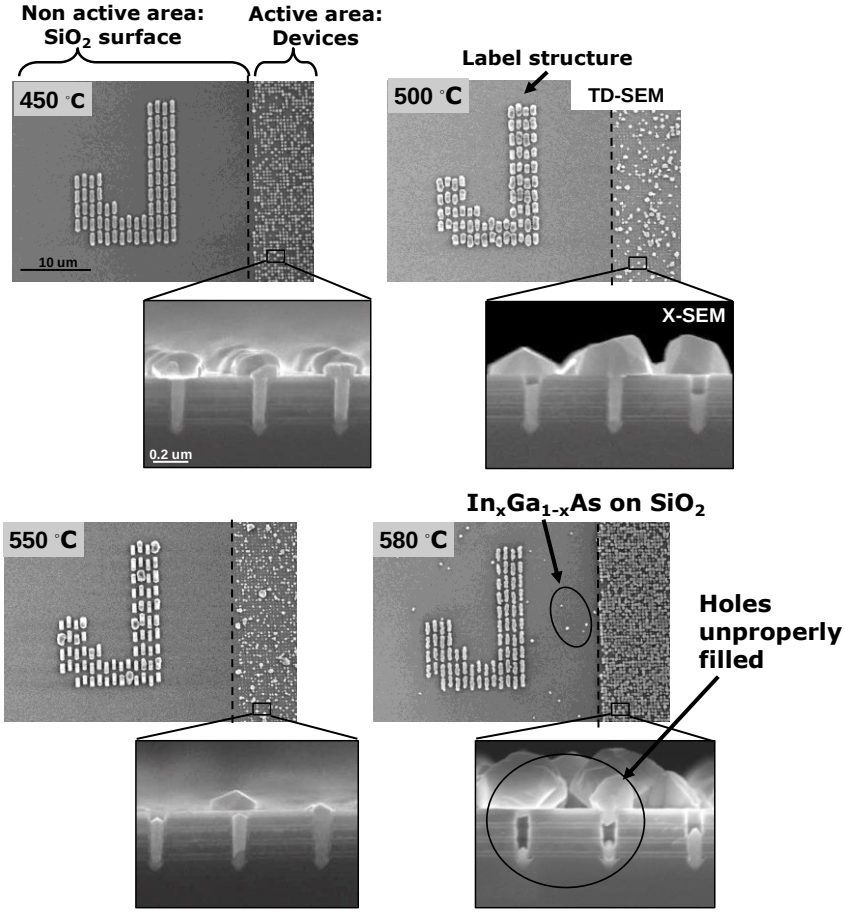


Figure 4.9: TD-SEM and X-SEM images on $In_xGa_{1-x}As$ channels with 65nm diameter (labeled with letter J), as a function of different T_{growth} and using TMGa as Ga precursor. Inspections are conducted on areas dedicated for SEM inspections. Selectivity is lost for $T_{growth} \geq 580$ °C.

The epitaxial growth of $In_xGa_{1-x}As$ is investigated as a function of different growth conditions. In Fig. 4.9 the III-V growth is analyzed for the case of TMGa precursor with different T_{growth}: TD-SEM inspections show good selectivity and absence of parasitic III-V deposition on the oxide area for deposition temperature ≤ 550 °C. On the other hand, a selectivity loss is observed at higher temperature (580 °C): parasitic deposition of $In_xGa_{1-x}As$ is observed on oxide area and the channel is closed at an early stage before it is fully filled. Higher T_{growth} leads to a more efficient precursors

decomposition and hence to a growth rate increase. As a consequence, the molecules that do not reach the memory holes start to nucleate on the oxide area. The hole filling capability is found to be temperature sensitive and dependent on the channel diameter: as the T_{growth} (chosen in a range not to cause selectivity loss) increases the percentage of filled devices is enhanced (Fig. 4.10.a). The channel filling capability also improves in larger holes (Fig. 4.10.b). However, the channel lengths are variable, as shown in Fig. 4.11: channels can end up undergrown or overgrown. This result may be explained as a consequence of process variations (e.g., different starting surfaces, roughness of the memory hole sidewalls and of the top surfaces), which lead to un-balanced material diffusion/transport into the memory holes and growth rate variations.

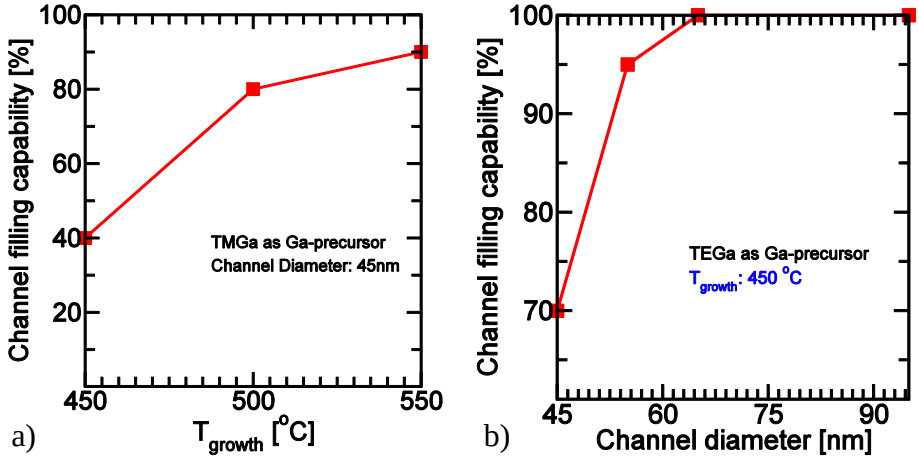


Figure 4.10: Channel filling capability as a function of: a) growth temperature and b) channel diameter. Holes down to 45 nm can be properly filled. The channel filling capability is extracted by inspecting ~500 devices via TD-SEM images.

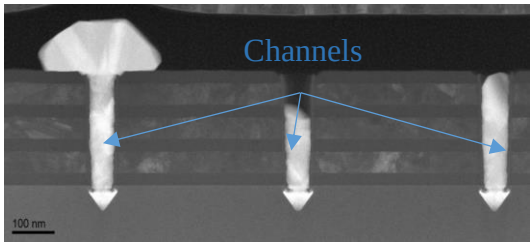


Figure 4.11: a) DF-STEM images on channels with a diameter of ~45 nm, by using TEGa as Ga precursor at 450 ˚C. Different channel lengths are observed.

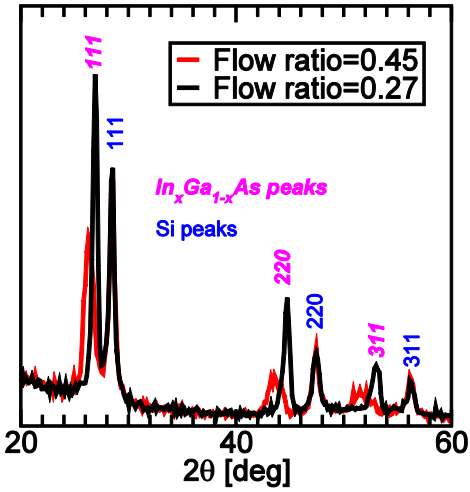


Figure 4.12: $In_xGa_{1-x}As$ XRD patterns for different flow ratio (In/In+Ga) by using TMGa as Ga precursor at 550 ˚C. Si peaks are detected from the poly-Si word plane. A shift of the $In_xGa_{1-x}As$ peaks is observed as the flow ratio changes, indicating a variation of $In_xGa_{1-x}As$ composition.

Initial overall channel composition screening is assessed through the $In_xGa_{1-x}As$ lattice parameter determined from XRD analysis and extracted by using Eq. (2.2) (section 2.3.1). The XRD diffractograms reported in Fig. 4.12 show multiple peaks, typically observed in polycrystalline materials, but this does not mean that the channels studied are also polycrystalline. Indeed, the XRD results are not collected on a single device, but are an average obtained on an area that includes the III-V overgrowth

(with different orientations) and structures (holes, trenches) with a wide range of dimensions.

Figure 4.13 reports the [In] extracted through the Eq. (2.3) (section 2.3.1), for different growth conditions: the incorporation efficiency of *In* increases by decreasing the T_{growth} for both TMGa and TEGa precursors. However, TEGa decomposes at lower T_{growth} as compared to TMGa [136], [137]. Furthermore, the [*In*] can be also tuned by modifying the flow ratio of the Ga and *In* precursors, and hence the amount of material that is transported into the chamber, while keeping the same T_{growth}: an increase of [In] can be achieved with larger In/Ga gas flow ratios.

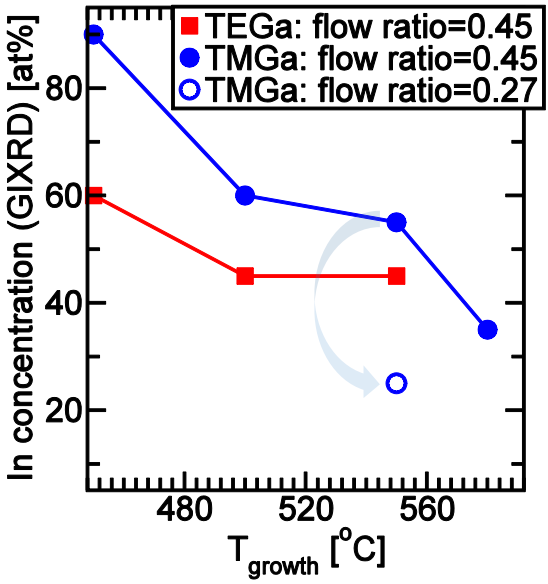


Figure 4.13: [*In*] obtained from XRD on samples of 3x3 cm^2 as a function of T_{growth}, Ga precursors and flow ratios. By changing the growth conditions, and the Ga precursors, different [*In*] can be obtained.

Energy Dispersive X-ray Spectroscopy (EDS) on STEM inspections are also conducted with the aim to evaluate the channel composition only on a device of interest. Figure 4.15 show the EDS mapping on a channel grown at 550 ˚C by using TMGa and a In/Ga gas flow ratio of 0.45. The obtained averaged composition are ~46 at % of *In* and ~52 at % of *Ga*. Those values are consistent with those obtained from XRD analysis on samples with the same growth conditions (Fig. 4.13).

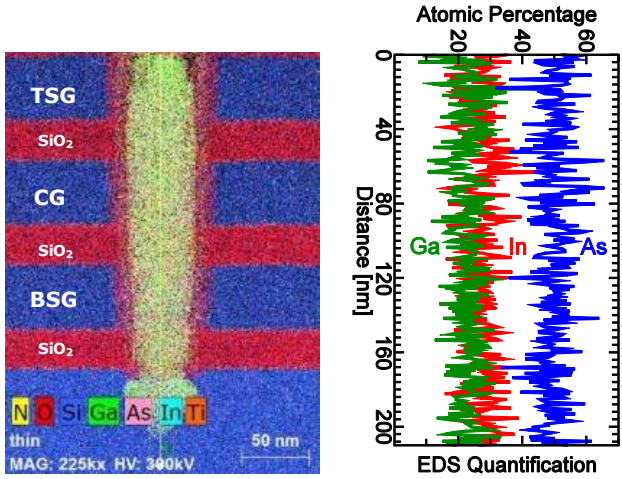


Figure 4.14: EDS-STEM mapping of a channel grown at 550 ˚C by using TMGa and a In/Ga flow ratio of 0.45. The normalized concentrations of *In*, *Ga* and *As* are reported and in average they correspond to ~$In_{0.46}Ga_{0.52}As$.

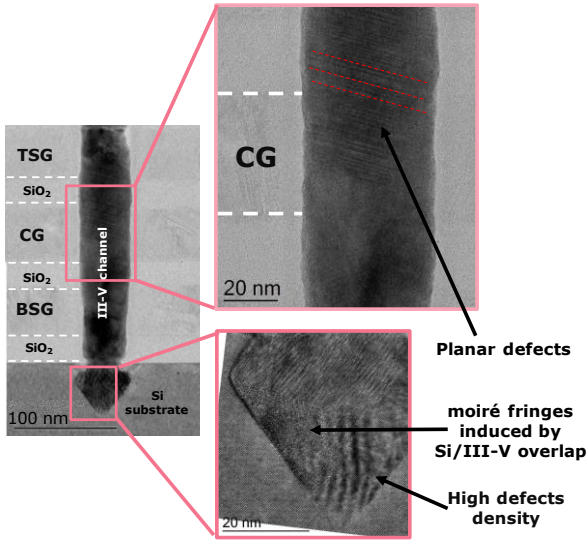


Figure 4.15: HR-TEM on individual channel grown at 550 ˚C by using TMGa and a In/Ga flow ratio of 0.45. Planar defects and threading dislocations are observed. Moiré fringes are caused by the overlap of Si and III-V.

The assessment of the channel quality is conducted by High Resolution TEM (HR-TEM) inspection, reported in Fig. 4.15: the channel is a single crystal. Misfit and threading dislocations are present at interface with the Si-substrate, where the growth is initiated. Those defects are caused by the large lattice mismatch between Si and III-V (~8% between Si and $In_{0.53}Ga_{0.47}As$) [139]. Furthermore, planar defects (stacking faults, nanotwins) are observed along the whole channel and they might be a consequence of an unoptimized III-V nucleation on the {111} Si surface or an insufficient surface preparation.

Out of the two *Ga* precursors and the different T_{growth} investigated for the III-V channel growth, the $In_xGa_{1-x}As$ recipes selected for the electrical characterization use TMGa and a T_{growth} of 550 °C. TMGa is preferred, since it is the most used *Ga* precursor, while the choice of T_{growth} equal to 550 °C is based on the promising results obtained (e.g., good channel filling capability). Furthermore two different cleaning routes are explored (HCl, and Cl_2) and three different [*In*] are obtained by changing the In/Ga gas flow ratio, as summarized in Table 4.2.

Recipe Name	Cleaning Route	$T_{cleaning}$ [°C]	In gas flow ratio (In/In+Ga)	Composition by X-Ray
H25	**HCl**	**900**	**0.27**	**$In_{0.25}Ga_{0.75}As$**
H45			**0.45**	**$In_{0.45}Ga_{0.55}As$**
H55			**0.53**	**$In_{0.55}Ga_{0.45}As$**
C45	**Cl_2**	**600**	**0.45**	**$In_{0.45}Ga_{0.55}As$**

Table 4.2: $In_xGa_{1-x}As$ recipes selected for the electrical characterization. The used Ga precursor is TMGa, while the T_{growth} is 550 °C. The composition is assessed through the $In_xGa_{1-x}As$ lattice parameter determined from the XRD patterns.

4.3.3 Metal Drain formation

In the reference Si integration flow, the source (S) and drain (D) junctions are diffused and implanted, respectively, in order to align the S with the bottom part of the BSG and the D with the top part of the TSG. The formation of both junctions requires temperatures higher than 1000 °C. Such temperatures are incompatible with $In_xGa_{1-x}As$. Therefore, to keep a low thermal budget, the S junction is skipped and metal is used as drain [140].

The metal drain consists of a stack of 10 nm thick titanium (*Ti*) deposited by physical vapor deposition (PVD), capped with 30nm thick TiN, deposited by ALD. *Ti* is used to reduce the contact resistance and as adhesion layer. ALD TiN is required to ensure proper connection to the overgrown channel. Moreover, a specially developed in-situ soft sputter etch is applied before metal deposition to enable a good contact between the channel and the drain.

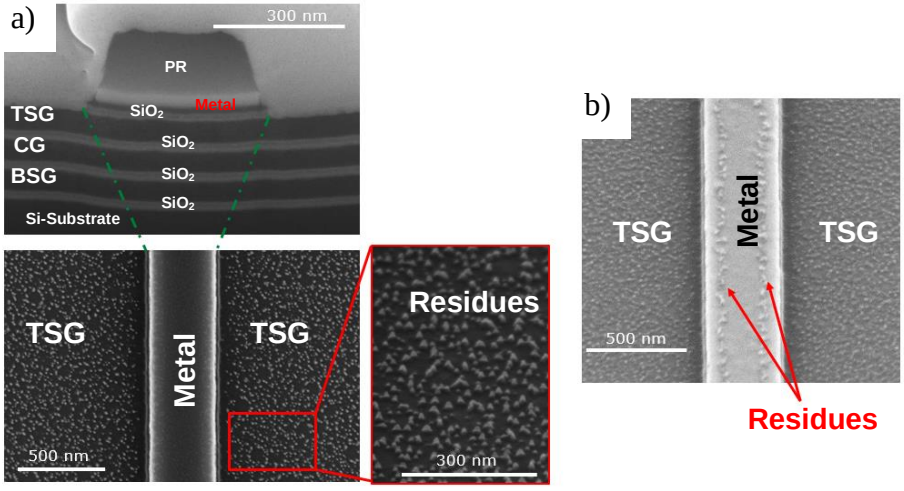


Figure 4.16: FIB and TD-SEM inspections conducted after metal drain etch. Sputtered residues are observed on top of a) the area not covered with PR and b) at the sidewalls of the metal.

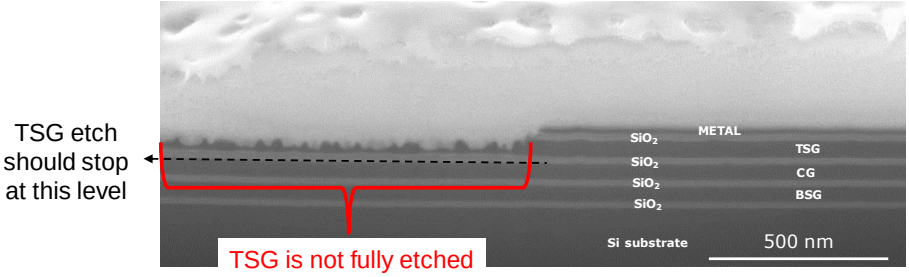


Figure 4.17: FIB inspection after TSG etch. Sputtered residues on the exposed area act as a mask, impeding the proper etch of the poly-Si TSG.

After the drain deposition, the process continues with the staircase patterning. Figure 4.16 shows the inspections conducted after the metal drain patterning: sputtered residues are present both on the regions not covered by the PR (e.g., TSG in Fig. 4.16.a) and at the sidewalls of the metal drain (Fig. 4.16.b). The residues on top of the metal drain can compromise the quality of the final drain contact, while the ones on top of the TSG act as a mask, impeding to etch properly the gates, as shown in Fig. 4.17, and hence to create the gates contacts.

In order to remove the by-products of the reactions acting as mask on the areas not covered by the PR, the drain etch recipe is adapted. Furthermore, to make sure that the residues on top of the metal are removed, an APM cleaning is used. Figure 4.18 shows the FIB inspection conducted just after the use of the optimized drain etch recipe: residues are no longer present on the TSG and the metal drain is cleaner than the case without extra cleaning (Fig. 4.16.b).

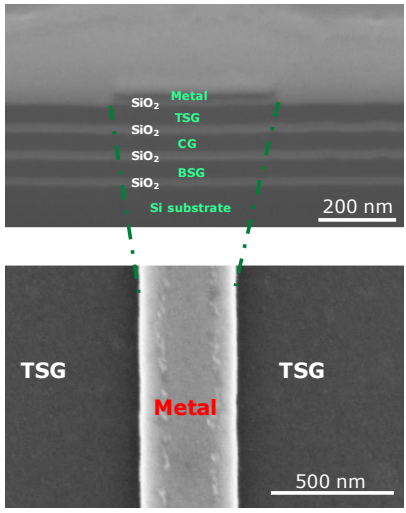


Figure 4.18: FIB and TD-SEM inspections after the optimization of the drain etch recipe; residues on top of the TSG are no longer visible, while on the metal drain have been reduced w.r.t. Fig. 4.16.b.

The formation of the contact also requires some adaptation; firstly, the oxide deposition for the isolation of the contacts is done at 400 ˚C instead of the typical 480 ˚C used in Si-process flow, to make it compatible with the thermal budget of both the III-V channel and the metal drain. For the same

reason, the sintering steps are removed from III-V process flow. Furthermore, since the metal drain is only 30nm thick, against the 180nm of the poly-Si drain, the oxide opening for the metal drain contact (Fig. 4.19.a) has also to be adapted. Figure 4.19.b shows the un-optimized contact opening: part of the drain is removed and it is almost cut at the edge. On the other hand, after the tuning of the recipe, the opening stops selectively on top of the metal drain, reducing the consumptions at the edges (Fig. 4.19.c). Finally, once the contact openings are created, the Metal 1 is deposited and patterned as in the Si-process flow.

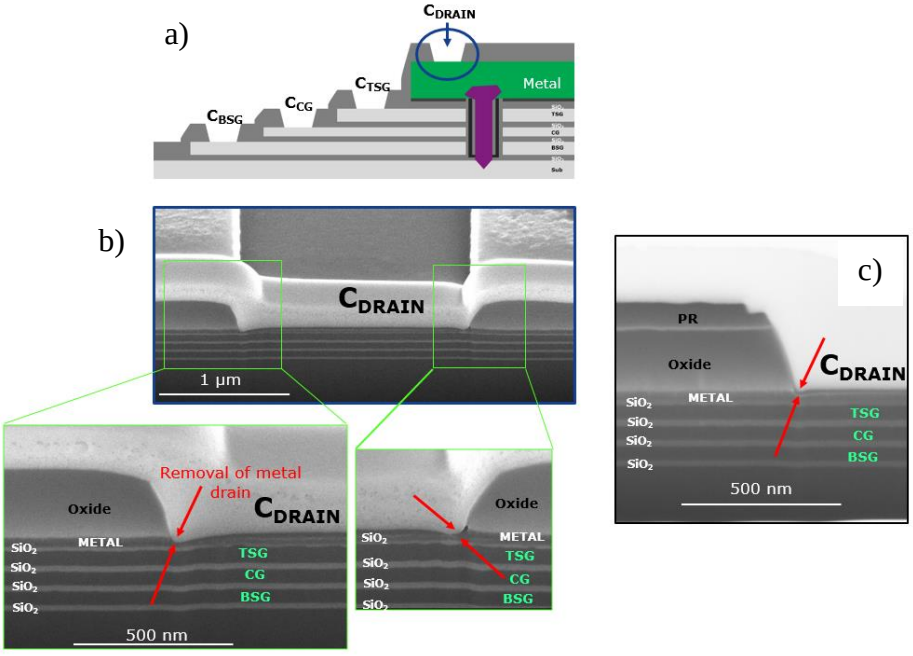


Figure 4.19: a) the contact opening which requires a tuning is highlighted with a circle in blue. FIB inspections after b) un-optimized contact opening and c) optimized contact opening.

4.4 Electrical characterization

I_D-V_G measurements are collected on poly-Si and epi-$In_{0.45}Ga_{0.55}As$ channels with a diameter of ~ 45nm. In order to limit the impact of the different nature and position of the S/D junctions with respect to the Si case, the electrical characterization is performed on the CG, as sketched in Fig. 4.1.b and Fig. 4.2.b. The side cells, TSG and BSG, are used to drive the junctions close to the CG via the application of a positive gate bias (5V).

4.4.1 III-V device operation

By performing I_D-V_G measurements on III-V channels, it is found that devices show large variability and populations with different behavior are distinguished, as shown in Fig. 4.20: some devices have low on current ($I_{on} \leq 1$ nA), others show high I_{on}, but they are not always well modulated.

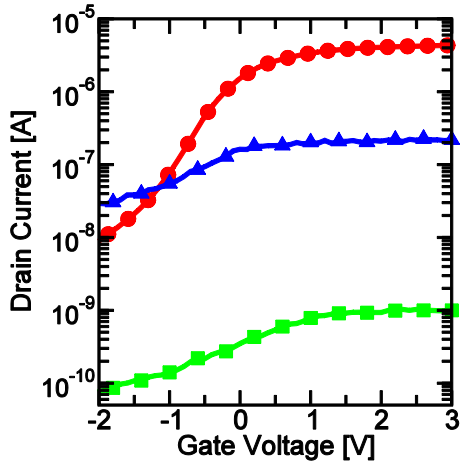


Figure 4.20: Typical I_D-V_G characteristics extracted from the different identified populations of III-V devices.

Table 4.3 summarizes the criteria used to assign devices to a certain population and 4 different typologies are distinguished.

Device Operation	Criteria to assign devices to a certain population		
	I_G [nA]	I_{on} [nA]	I_{on}/I_{off}
Gate Leakage	≥ 1		
Low Current	< 1	≤ 1	
Unmodulated Current	< 1	>1	≤ 100
High Current	< 1	>1	>100

Table 4.3: III-V devices operation based on the $I_{G,}$ the I_{on} and the ratio between I_{on} and the off current (I_{off}). Devices with high I_G (which can be originated by the damage of the CG, TSG or BSG during the integration) are immediately removed from the analysis.

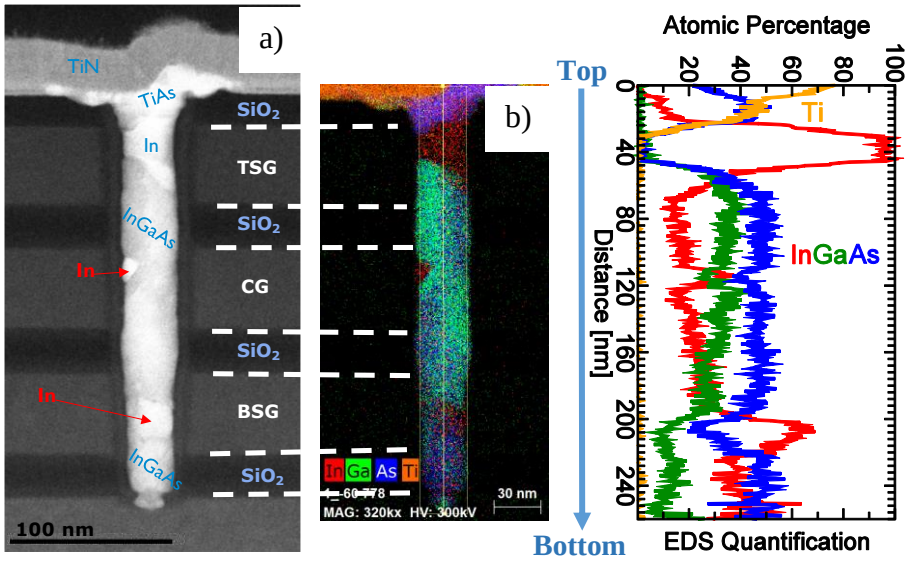


Figure 4.21: a) HAADF-STEM and b) EDS map on a device with low I_{on}. Composition variations are observed along the memory string.

In order to correlate the different devices operations with the III-V channel morphology, TEM and EDS analysis are conducted on each typology of observed devices. Figure 4.21.a shows the HAADF-STEM on device with low I_{on}: different contrasts are observed along the channel, symptomatic of material variations, as corroborated by EDS map in Fig. 4.21.b. Drift of the composition and In segregation are present along the memory string, while a *Ti*/*As* mixture is observed next to the metal drain;

un-modulated devices (not shown), have similar composition variations, but the *In* segregation is also placed in the center of the CG transistor. On the other hand, devices with modulated and high current are characterized by an uniform composition along the channel, as shown in Fig. 4. 22.

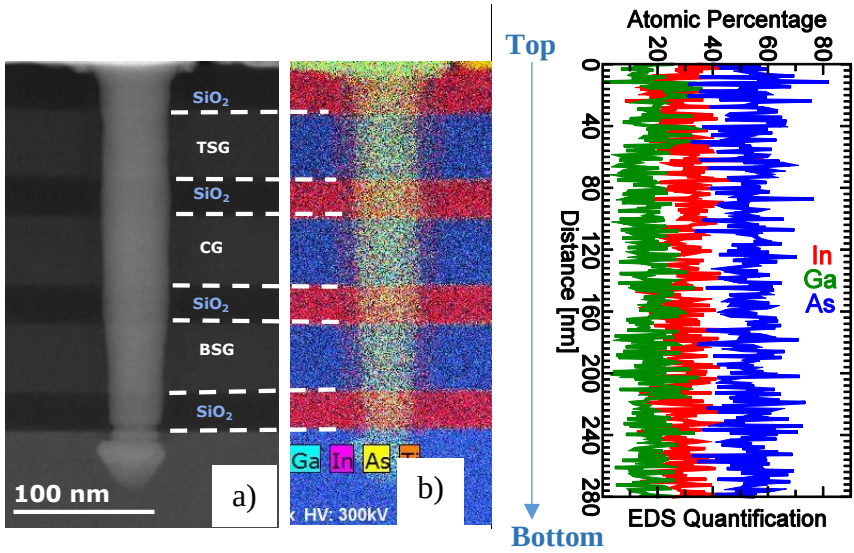


Figure 4.22: a) HAADF-STEM and b) EDS-STEM mapping on devices with modulated high I_{on}. The composition along the channel is constant.

The results obtained by TEM and EDS indicate that the integration of the III-V channels is not fully optimized and the channel variability has a strong impact on the electrical performance. Therefore, in the next sections, the electrical analysis will be conducted only for devices with modulated and high I_{on}.

4.4.2 I_D-V_G characteristics and mobility extraction

Figure 4.23 compares the typical I_D-V_G of $In_{0.45}Ga_{0.55}As$ (H45) and two different flavors of Si channels (FA-Si and LTA-Si): III-V outperforms all the other channels, even if it presents a strong saturation of I_{on} and higher I_{off}. Furthermore, the apparent μ of H45 and FA-Si channels are also extracted. Generally, an accurate channel μ is extracted by using the so-called *dR/dL* method [141], [142] expressed by Eq. (4.1):

$$\mu = 1/\left(W Q_{inv} \frac{dR_{total}}{dL_{eff}}\right) , \quad (4.1)$$

where W is the channel width, Q_{inv} is the inversion charge extracted by integrating the split C-V measurements, and dR_{total}/dL_{eff} is determined by plotting the measured total device resistance as a function of the effective channel length (L_{eff}), and taking the slope of the curve. The advantage of this method is that the mobility can be extracted without knowing the exact value of R_{total} and L_{eff}.

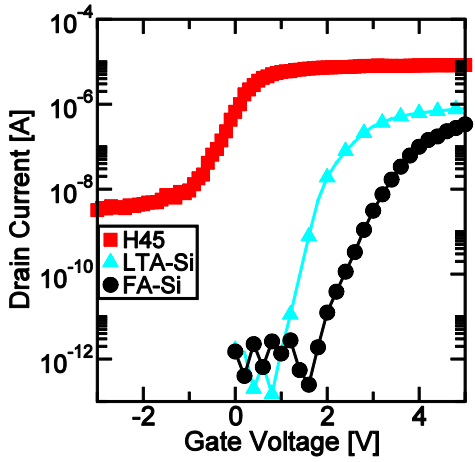


Figure 4.23: Typical I_D-V_G for channels with ~45 nm diameter. Electrical characterization is performed by sweeping the CG up to 5 V while keeping 5 V at side gates and 0.5 V at the drain.

However, the maskset adopted does not have dedicated structures for the extraction of an accurate channel μ (e.g., channels with different lengths, and structures for *C-V* measurements). Therefore, a first order μ estimation is done; it consists in approximating the string in one long transistor, by neglecting the series resistance in the IGS regions and at the source/drain contacts. As the approximations should affect both channels in a similar way, a comparison between *Si* and III-V can still be done. Thereafter, the μ extraction is conducted from the equation of the maximum g_m (g_{mMAX}) of the MOSFET in the linear regime [111], as descibed by Eq. (4.2):

$$\mu = g_{mMAX} L^2 / V_{DS} C_{ONO} \ , \tag{4.2}$$

where L is the string length, measured between the BSG and TSG, C_{ONO} is the capacitance computed as the series of the cylindrical capacitors of the ONO layers, assuming the thicknesses reported in section 4.2, while g_{mMAX} is extracted after the smoothing of the I_D-V_G curves, as shown in Fig. 4.24. I_D-V_G curves are performed by biasing the drain at 100 mV, to guarantee the extraction of the g_{mMAX} in the linear regime (Fig. 4.24.a); then, the curves are smoothened (Fig. 4.24.b) by using a Gaussian Kernel filter [143] in Matlab [144] and the g_{mMAX} is finally extracted.

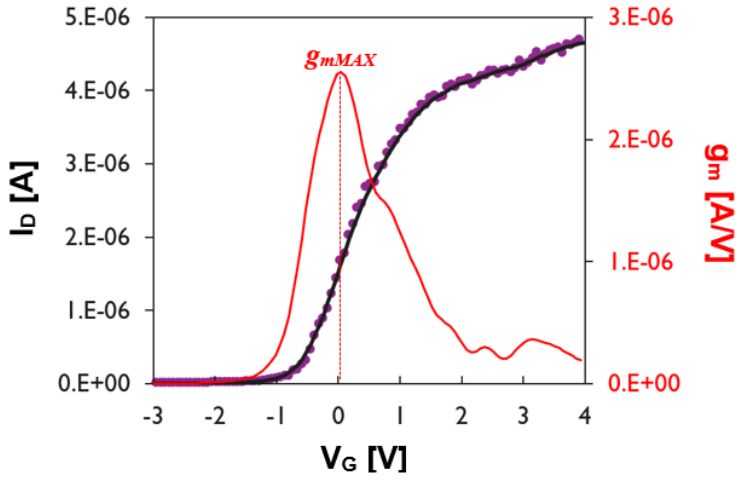


Figure 4.24: Procedure to extract the g_{mMAX}. The measured I_D-V_G is filtered and the derivative of the smoothened curve is calculated; the maximum value of the derivative represents the g_{mMAX}.

III-V mobility is capable to overcome the one of FA-Si, as shown in Fig. 4.25: the median value of μ in III-V channels is ~15 times higher than the FA-Si one and the values above 1 σ exceed 100 cm^2/Vs.

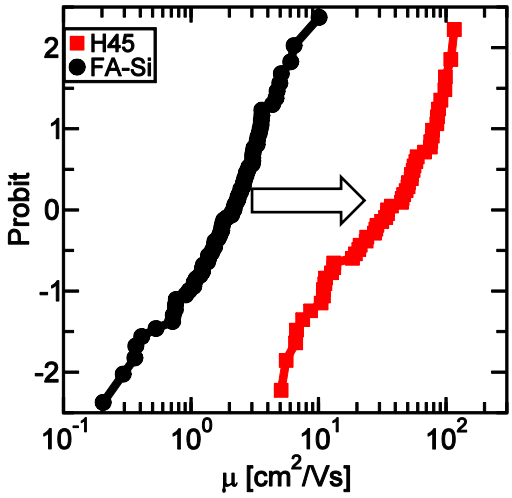


Figure 4.25: Statistical distribution of the apparent value of μ extracted for H45 (see Tab. 4.2) and FA-Si with channel diameter of ~45 nm. III-V channel has better μ as compared to FA-Si.

To investigate the conduction properties of the III-V and FA-Si channels without the influence of the gates and of the source/drain contacts, Scalpel scanning probe microscopy (SPM) technique is applied. Scalpel SPM is based on the conventional 2-D conductive atomic force microscopy (C-AFM) [145], [146]. Additionally, it has the capability to probe in 3-D with nm precision, thanks to a slice-and-view methodology based on the physical removal of material during the scanning. Therefore, this technique is suitable for the 3-D characterization of ultra-confined volumes like our vertical channels. Details on the technique are reported in [147], [146].
Figure 4.26.a shows the Scalpel SPM procedure in our channels: a conductive diamond tip is used to induce a controlled material removal into the memory hole at each consecutive C-AFM scan. During the material removal the current maps of the vertical channel at different heights are collected, as reported in Fig. 4.26.b. Once all the C-AFM slices are acquired, they are stacked and interpolated to obtain a 3-D tomogram. Specifically, for our devices this approach allows a direct access to the channel material, which can be used to compare various process conditions or channel materials.

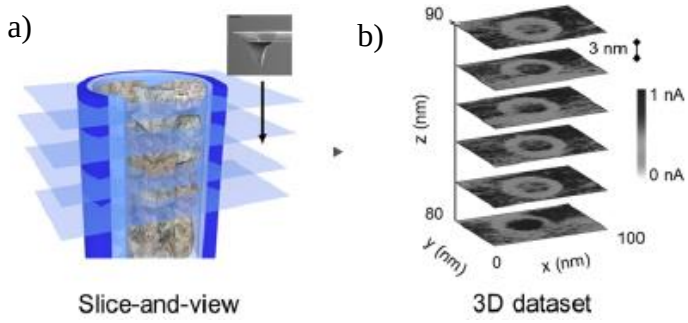


Figure 4.26: Schematic of the Scalpel SPM procedure. a) The diamond tip is used to dig into the vertical channel at each consecutive C-AFM scan. b) Stacked representation of the 2-D C-AFM slices at different heights of the channels prior to the 3-D interpolation. The average space between each slice is ~3 nm.

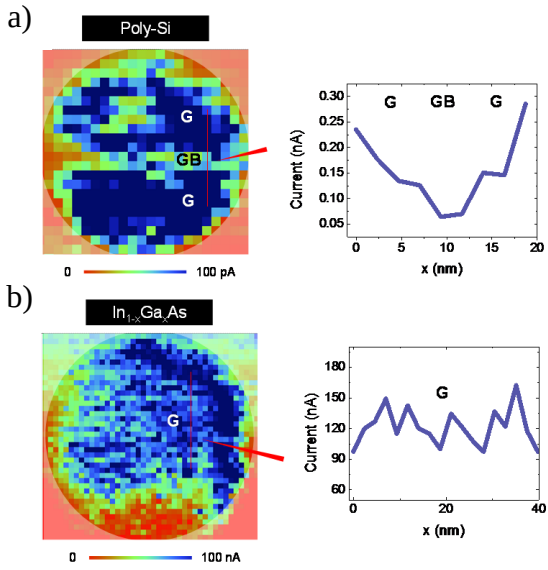


Figure 4.27: 2-D C-AFM current maps for a) FA-Si, and b) $In_xGa_{1-x}As$ channels; a network of lowly conductive regions, associated to the grain boundaries (GBs), is visible in the cross-section of FA-Si, while the III-V channel presents a higher average conductivity and localized area with enhanced current (in blue).

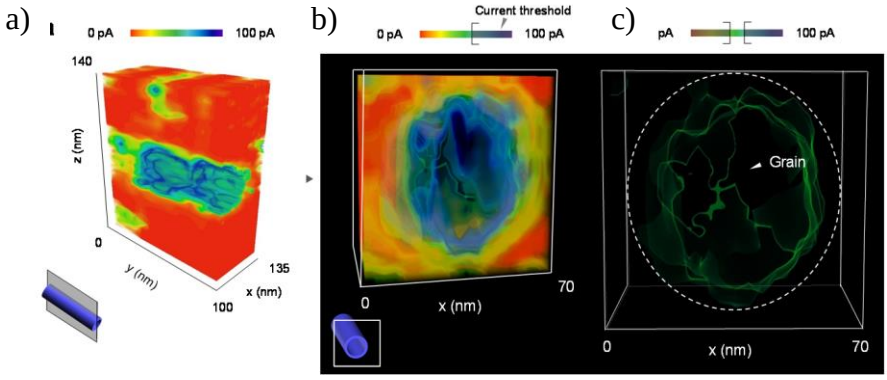


Figure 4.28: a) tomographic reconstruction of FA-Si channel. b) A fixed threshold current is applied in order to highlight regions with different conductions. c) The tomogram is filtered to suppress the high current contribution thus revealing the network of GBs inside the FA-Si channel.

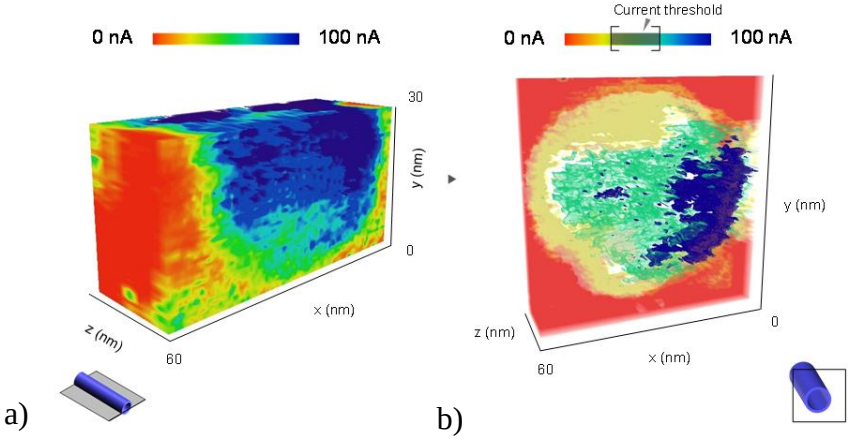


Figure 4.29: a) Tomographic reconstruction of the $In_{1-x}Ga_xAs$ channel. b) By filtering the tomogram, highly conductive domains with a size of ~20 nm appear (blue area) while GBs are not visible.

Figure 4.27 compares the current maps for FA-Si and $In_xGa_{1-x}As$ in a C-AFM slice: the average current flowing inside the $In_xGa_{1-x}As$ channel (Fig. 4.27.b) shows an increase of a factor 1000 with respect to the FA-Si one (Fig. 4.27.a). Different grains (indicated with G) are observed in FA-Si.

Interestingly, the GBs in FA-Si creates regions with limited conduction running through the channel, as visible in the cross-sectional cut of Fig. 4.27.a. After the interpolation of the 2-D C-AFM slices (Fig. 4.28.a, and 4.29.a), the different conductive areas inside the FA-Si channels are more clear by applying an appropriate threshold in the current tomogram, as shown in Fig. 4.28.b. On the other hand, the GBs, which present reduced mobility, can be revealed by a bandpass filter applied to the tomogram (Fig. 4.28.c): the presence of GBs is consistently observed for the FA-Si samples. For $In_xGa_{1-x}As$ channels (Fig. 4.29.a) the same procedure leads to the presence of 20nm wide areas with enhanced conductivity, likely due to the presence of In segregation (highlighted in blue in Fig. 4.29.b), also detected by EDS map in Fig. 4.20.b. However, the conduction of $In_xGa_{1-x}As$ largely exceed the one in FA-Si, also in the areas where the In clusters are not present. Indeed, the threshold current applied on $In_xGa_{1-x}As$ channels is in the range of nA, contrary to the pA used for FA-Si ones.

4.4.3 Impact of [*In*] on the electrical characteristics

Figure 4.30 shows I_{on} and I_{off} distributions of all the available $In_xGa_{1-x}As$ recipes (see Table 4.2). As expected, independently of the used surface preparation, devices C45 and H45 show comparable I_{on} and I_{off} values. The higher the [*In*], the larger both currents are; the [*In*] increase results in a reduction of the band gap, leading to higher mobility, and hence higher I_{on} [13]. On the other hand, lower band gaps facilitate the Band To Band Tunneling (BTBT) mechanisms which cause an I_{off} increase [148]. In addition, both I_{on} and I_{off} can be affected by Si diffusion, which acts as n-type dopant [149], from the substrate into the channel, as expected to happen during $In_xGa_{1-x}As$ growth [150], [151]. However, the variations of I_{off} and I_{on} between H25, with the lowest [*In*], and H55, with the highest [*In*], are not in the same order: H55 devices show only ~2 orders of magnitude higher I_{on} than H25, but ~5 orders of magnitude higher I_{off}.

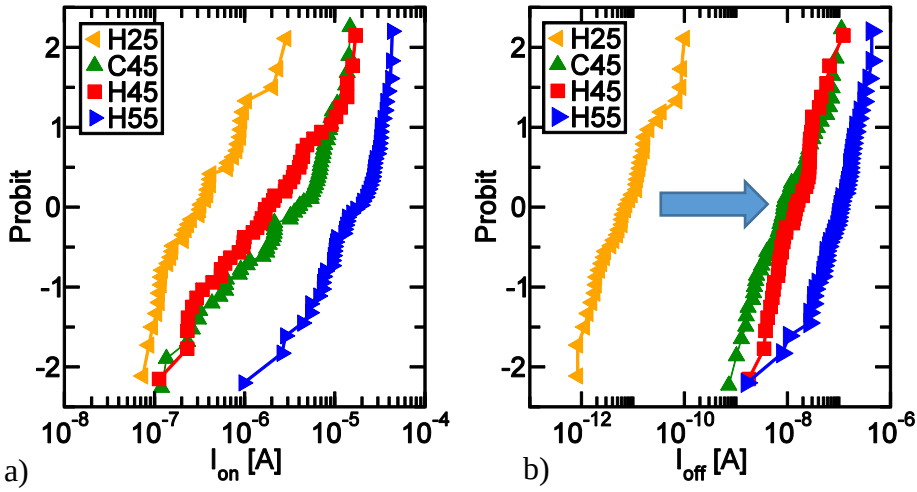


Figure 4.30: Distribution of: a) I_{on} at fixed V_{ov} = 2 V, and b) I_{off} for different surface preparations and [*In*] (see Table 4.2). The higher the [*In*], the larger both I_{on} and I_{off} are.

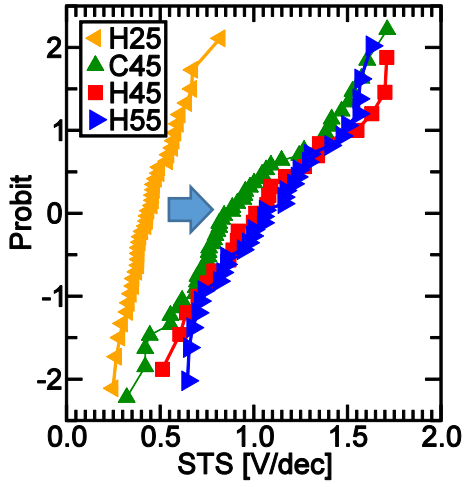


Figure 4.31: Distribution of the STS for different surface preparations and [In] (see Tab. 4.2). Devices H25 have steeper and lower *STS*, indicating better channel/TuOx interface.

One of the factors responsible for the I_{off} increasing might also be the trap assisted tunneling (TAT) mechanism, due to the presence of defects at

the interface [152]–[154]. Figure 4.31 shows the *STS* of devices with different [*In*] and it is shown that H25 have the lowest *STS* values and the narrowest distribution. This result is a clear indication of less defective interface, leading to a reduction of the I_{off}.

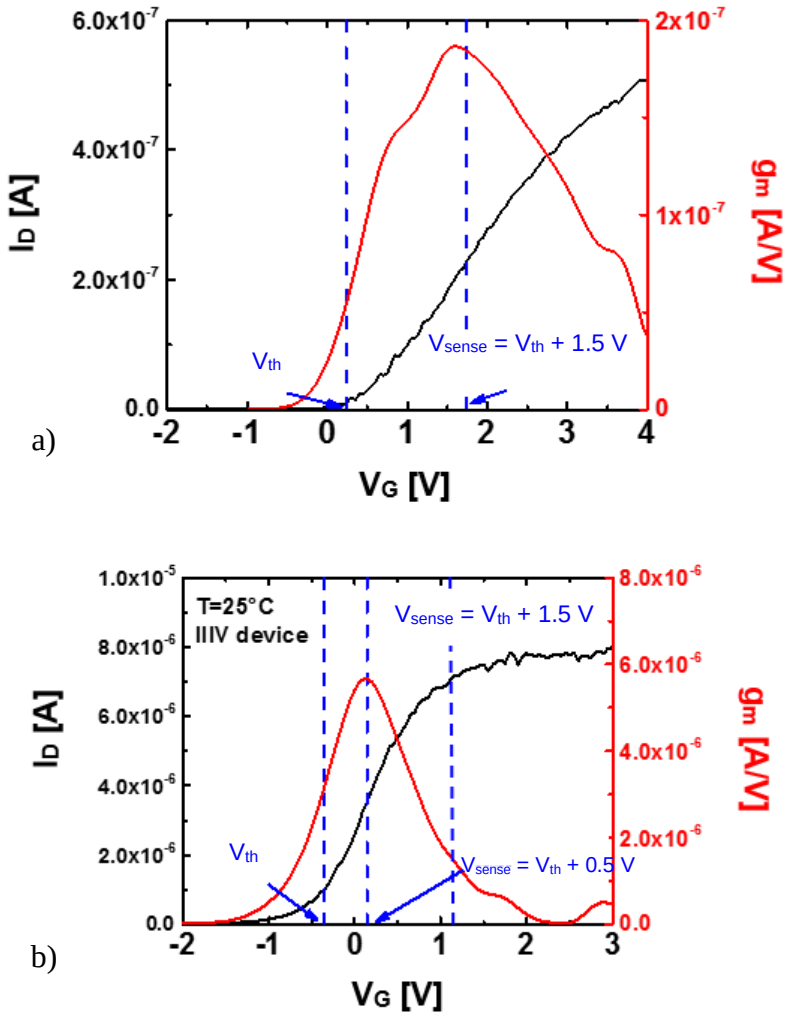


Figure 4.32: g_m extraction by using the method discussed in (3.6) for a) FA-Si and b) III-V devices. The g_m of the III-V devices cannot be extracted at the same value of V_{sense} as the one used for FA-Si, since it is affected by series resistance; therefore a lower value has to be chosen.

The conduction properties of our channels are investigated by extracting the g_m from I_D-V_G curves recorded at a slow V_G ramp rate, with high resolution (1 mV/step), following the procedure described in (3.6).
As for the case of Epi-Si and Epi-$Si_{1-x}Ge_x$ (STRATO test vehicle in 3.7), the g_m of FA-Si is extracted at $V_{sense} = V_{th} + 1.5$ V, as shown in Fig. 4.32.a. The same V_{sense} cannot be used for the III-V channels, since the I_D-V_G starts to saturate, underestimating g_m (Fig. 4.32.b). In order to properly extract g_m in III-V channels, a lower V_{sense} ($V_{sense} = V_{th} + 0.5$ V) is used. Note that in Fig. 4.32 the chosen values of V_{sense} allows to extract g_m close to the g_{mMAX}. In Fig. 4.33 the g_m of all the available $In_xGa_{1-x}As$ recipes (see Table 4.2) are benchmarked against the one of FA-Si: in the III-V channels the conduction is not affected by the different cleaning routes, as already observed in Fig. 4.30, and it improves as the [*In*] increases. Devices H25 only show a marginal improvement in the conduction over the *Si*-reference. Instead, devices H45, which are comparable to C45, and devices H55, allow to outperform FA-Si by up to 2 orders of magnitude.

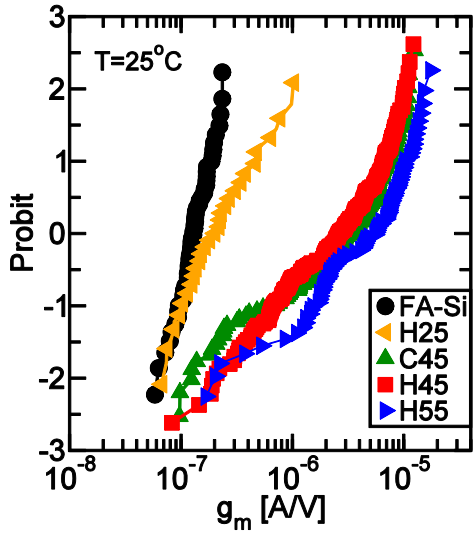


Figure 4.33: g_m distribution for FA-Si and $In_xGa_{1-x}As$ channels with three different [*In*] (Table 4.2). As the [*In*] increases the g_m is improved; devices H25 show a g_m comparable to FA-Si channels.

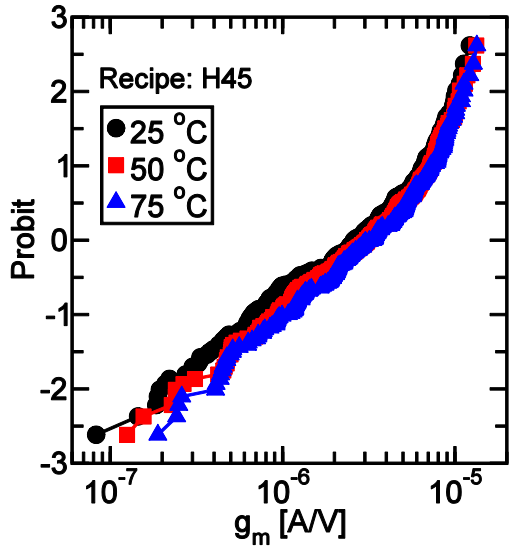


Figure 4.34: g_m distribution of recipe H45 (Table 4.2) as a function of temperature. Contrary to single crystal channels, g_m increases with temperature.

As already noticed in epi-Si channels in (3.6), both H45 and C45 show bimodally distributed g_m, as shown in Fig. 4.33: this behavior is indicative for non-perfect, (e.g., defective) crystal growth. The defective nature of the III-V channel is observed in HR-TEM (Fig. 4.15) and it also corroborated by the temperature dependence of g_m in Fig. 4.34. Indeed, contrary to the ideal single-crystal channel, these devices present an increase of g_m with temperature, also observed in H25 and H55 (not shown). As discussed in (3.7), this phenomenon is generally associated with thermionic emission over defect-induced barriers. Therefore, a positive E_{ACT} of the g_m is extracted for most of the III-V devices (see Fig. 4.35) by using Eq. (3.3).

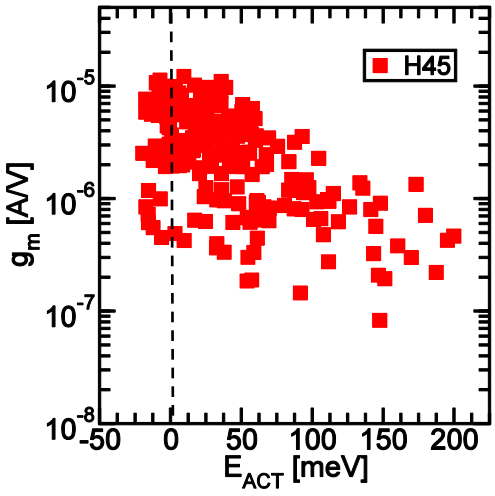


Figure 4.35: Correlation between g_m and its E_{ACT} for H45 samples; high spread is observed and most of the devices show a positive E_{ACT}, indicating that the conduction is hampered by channel variability and defects.

The correlation between the E_{ACT} and the mean value of g_m ($<g_m>$) is finally shown in Fig. 4.36 for the case of $In_xGa_{1-x}As$ with different [In], several flavors of poly-Si [76], [155], [156] and epi-Si and epi-$Si_{1-x}Ge_x$ channels. The different types of poly-Si channels show a strong correlation: the higher the average g_m is, the lower the E_{ACT} is, indicating that the conduction in poly-Si channels is dominated by the number of grains (and hence their configuration) and by percolation paths [157]. Epi-Si and epi $Si_{1-x}Ge_x$ channels, are also in the same trend-line; although those channels are not perfectly epitaxially grown and contain planar defects, their conduction properties are improved. Independently of the [*In*], $In_xGa_{1-x}As$ is outside of the Si trend-line, and its E_{ACT} decreases by increasing the [*In*], most probably because the effect of the higher mobility prevails over the channel defectivity. H45 and H55 confirm to have superior conduction properties compared to poly-Si and epi-Si channels, even in presence of an unoptimized process.

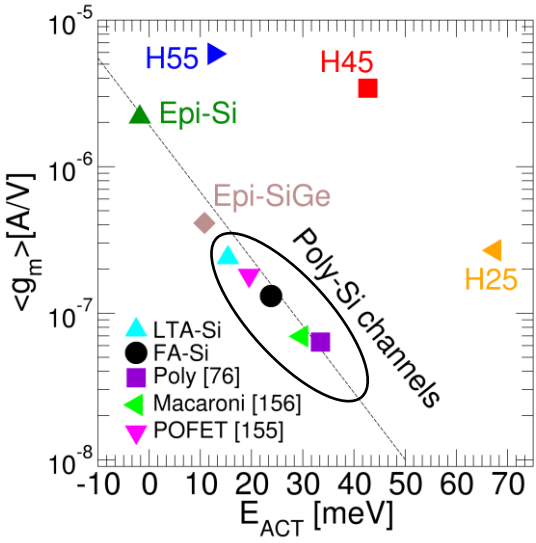


Figure 4.36: Correlation between $<g_m>$ and the activation energies for several flavors of poly-Si, epi-$In_xGa_{1-x}As$ with different [*In*] (Table 4.2), epi-Si and epi-$Si_{1-x}Ge_x$ channels.

4.5 ONO integrity analysis

In (4.3.1) we have seen that the surface preparation conducted before the channel growth could consume the TuOx. To investigate the thickness, as well as the quality of the TuOx, several measurements are performed and described in detail in the next sections; the assessment of the TuOx thickness is done through the analysis of the *P/E* performance. Long-term retention tests, which are sensitive to both the thickness and the quality of the SiO_2, are also carried out and the analysis of the TuOx quality is further supported by post program discharge (PPD) measurements.

4.5.1 Evaluation of the TuOx consumption

The assessment of the TuOx consumption is done by performing long-term retention measurements at room temperature on H45 ($In_{0.45}Ga_{0.55}$

with HCl route) and FA-Si devices. The evolution of the stored charges is evaluated as a function of retention time at room temperature. The CG of ~20 devices are programmed with 100 μs program pulse, to achieve ΔV_{th} = 4 V from their fresh state. The side gates (TSG and BSG) are kept at 5 V. The V_{th} is monitored for two weeks at regular intervals: device H45 show a charge loss of ~1 V after 1 day, while the loss in FA-Si is ~250 mV, as shown in Fig. 3.37. This result indicates that the TuOx in III-V channel is thinner.

To extract the amount of the TuOx consumption on the III-V devices, caused by the HCl-based surface preparation, simulations of the measured retention characteristics are carried out. Simulations are performed by using a 2-D charge trapping memory simulator, designed to reproduce *P/E* and retention transients [158].

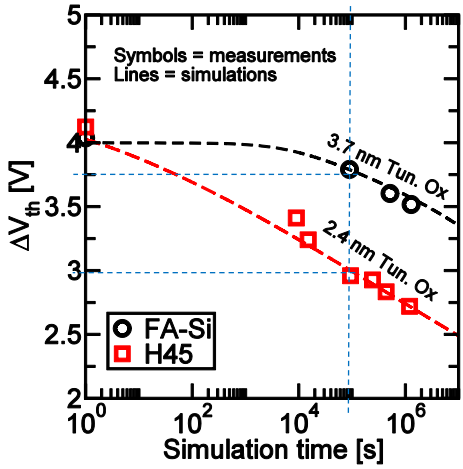
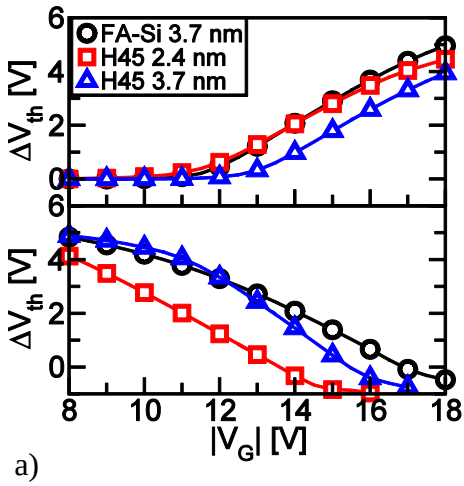
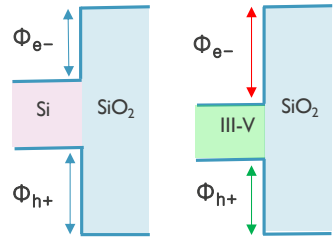


Figure 4.37: Simulation of the measured retention characteristics at room temperature for H45 and FA-Si channels. H45 show a loss of ~1 V after 1 day due to a 1.3 nm thinner TuOx than the one in FA-Si.

From simulations results (Fig. 4.37), it is found that the TuOx in III-V devices with HCl route is ~1.3 nm thinner than FA-Si (2.4 nm against the 3.7 nm of thick TuOx in FA-Si). Even if the TuOx in III-V devices was thickened by ~1.5 nm (Table 4.1), to compensate for possible consumption, still part of it was consumed.





b)

	Si	*III-V*	*SiO_2*
Electron affinity (eV)	4.05	4.44	0.95
Band gap (eV)	1.12	0.84	9
P Φ_{e-} (eV)	***3.1***	***3.49***	
E Φ_{h+} *(eV)*	***4.78***	***4.67***	

Figure 4.38:a) Simulated *ISPP*/*ISPE* for H45 and FA-Si channels; the red and black curves are the fitting of the measured *ISPE* and *ISPP* while the blue curve is simulated by using the same parameter used for the red one but by considering the TuOx on target. b) Band diagrams of the systems III-V ($In_{0.45}Ga_{0.55}As$)/TuOx and Si/TuOx. The barrier heights seen by electrons (ϕ_{e-}) and by holes (ϕ_{e-}) are calculated by considering the electron affinity and the band gap values reported in [103].

ISPP and *ISPE* (introduced in 1.1.2) are performed and reported as the medians of the ΔV_{th} relative to the fresh state acquired on ~20 devices. Program is conducted on the central cell, starting from the fresh state using the conditions mentioned above. Erase is instead performed immediately after the device is programmed using 1 ms erase pulses and maintaining side gates at -10 V. To compare how the III-Vs behave with and without a TuOx on target, the measured *P/E* characteristics are then used to calibrate the model for simulations. The simulated *P/E* curves are reported in Fig. 4.38.a: due to the thinner TuOx, H45 show comparable program speed and faster erase than FA-Si. Once accounting for ~1.3 nm thinner TuOx, H45 presents slower program speed and slightly faster erase than FA-Si; this result is originated by the band offsets between the systems III-V/TuOx and Si/TuOx, as shown in Fig. 4.38.b.
When comparing the measured *P/E* characteristics of H45 and FA-Si with the ones of C45 (which uses Cl_2 instead of HCl as surface preparation (Table 4.1)), devices C45 show slower program and poor erase (Fig. 4.39).

These results are not in line with the simulated characteristics when the TuOx is on target (Fig. 4.38) and they are a clear indication of a thicker oxide as deposited (see Table 4.1); this confirms that the Cl_2 route does not consume the oxide and a preventive thickening of such layer is not required.

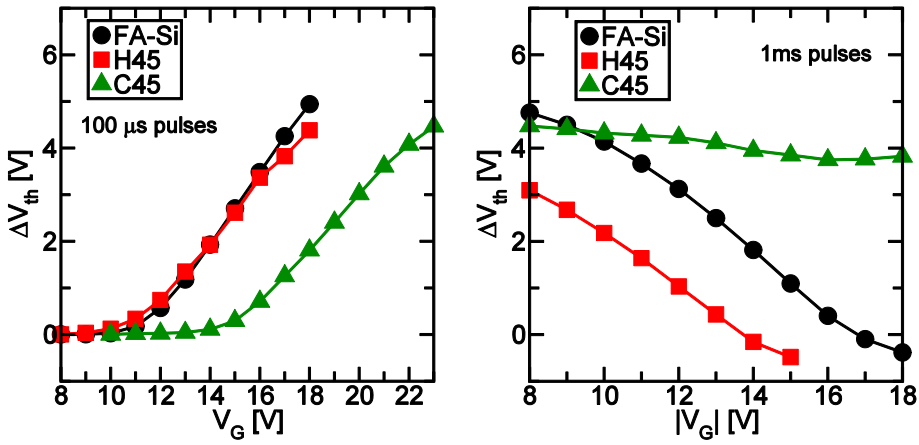


Figure 4.39: Measured *ISPP*/*ISPE* for H45, C45 and FA-Si channels. Devices H45 shows similar program and faster erase as compared to FA-Si, symptomatic of a thinner TuOx, while C45 has slower *P/E*, as a consequence of a thicker oxide.

Therefore we can conclude that the HCl-based surface preparation is an unreliable approach and not suitable for future integration, since the amount of consumed TuOx is difficult to control. Cl_2 route instead is promising as it is able to preserve the oxide thickness.

4.5.2 Evaluation of the TuOx quality

Long-term retention tests are performed at room temperature, as described in (4.5.1). Since III-V devices with Cl_2 route as surface preparation present thicker TuOx, they are not always able to reach a ΔV_{th} = 4 V from the fresh state. Therefore a lower program target is chosen (e.g., ΔV_{th} = 3.5 V).

Retention of devices C45 (Table 4.2) is improved with respect to that of H45 (Table 4.2), but despite our expectations, provided by the thicker

TuOx, a significant charge loss is still observed, as shown in Fig. 4.40. Contrary to the *Si* process flow, III-V one does not include any high temperature step after the channel formation. If we introduce a bake at 625 °C for 3 min to the recipe C45 just after the channel formation, a reduction of the charge loss is observed. This suggests that the retention loss is dominated by TuOx defects which can be, at least partially, annealed by subsequent thermal treatment.

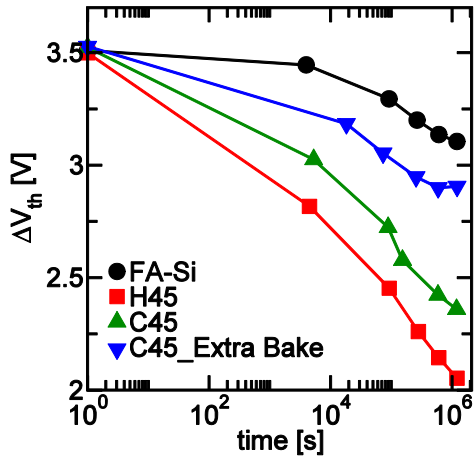


Figure 4.40: Long-term retention for poly-Si and $In_{0.45}Ga_{0.55}As$ channels with HCl or Cl_2 route, and with and without bake after the channel formation (C45, C45_Extra Bake). Even if C45 has thicker TuOx as compared to FA-Si and H45, a significant charge loss is still observed; the retention can be improved introducing a bake after the channel formation.

To further corroborate the defective nature of the TuOx, investigations with PPD measurements are conducted. PPD allows to monitor a fast transient ΔV_{th} after programming, related to discharging phenomena due to the presence of near-interface TuOx defects; during programming such defects are charged, but due to their vicinity to the substrate, they are not capable of retaining their charge for more than a few ms [159], leading to a charge loss. The PPD technique is shown in Fig. 4.41: it consists in programming the CG by applying a V_{pgm} of 16 V for 10 ms, after an initial I_D-V_G measurement. After the program pulse, the CG is immediately biased at a V_{sense}, which is chosen close to the value of the V_{th} expected after the

program pulse. Afterwards, the I_D measured at V_{sense} is compared with the I_D performed prior to the program; assuming that the program does not degrade the *STS*, the ΔV_{th} can be extracted. The evolution of the ΔV_{th} is then assessed by alternating the CG between a waiting voltage (V_{WAIT}), which is equal to 0 V and the V_{sense}. During the whole PPD measurement both the TSG and the BSG are kept at 5 V, while 0.5 V is applied on the drain. More details on the technique can be found in [159].

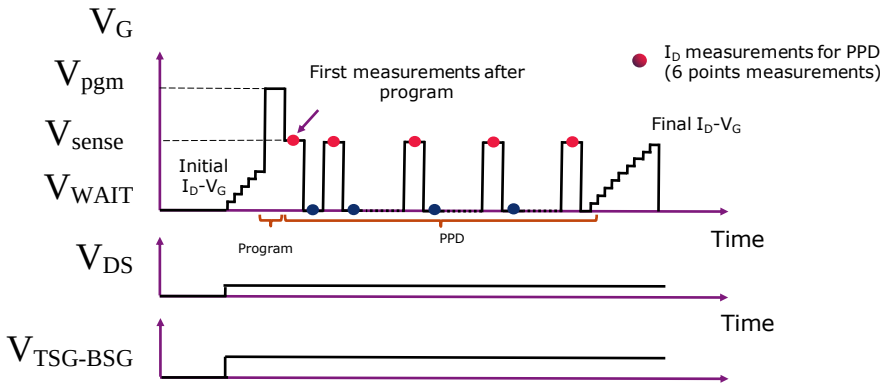


Figure 4.41: Schematic of the PPD measurement on the CG. After the program pulse at V_{prg}, V_G is immediately brought at V_{sense} to assess the programmed state. Then, V_G is alternated between V_{WAIT} and V_{sense}, while the drain, the TSG and the BSG are kept at a fixed voltage for the entire measurement [159].

Figure 4.42 reports the PPD measurements performed on FA-Si devices and $In_{0.45}Ga_{0.55}As$ channels with Cl_2-based cleaning (C45): uncycled FA-Si devices do not show any ΔV_{th} shift (e.g., charge loss) for the entire PPD duration, indicating a low defectivity in the TuOx [159]. On the other hand C45 shows an abrupt charge loss. This loss is comparable to the one observed on FA-Si devices with a degraded TuOx after100 *P/E* cycles. Moreover, in agreement with long-term retention, PPD also shows that extra annealing can improve the quality of TuOx, indicated by the reduction of the ΔV_{th} shift.

The TuOx defectivity represents a real bottleneck for the memory performance. Such defectivity might be generated by the epi III-V growth as well as by the surface preparation. Therefore, in Chapter 5 dedicated

experiments and treatments are carried out to better assess the origin of the TuOx defectivity and to try to improve the TuOx quality.

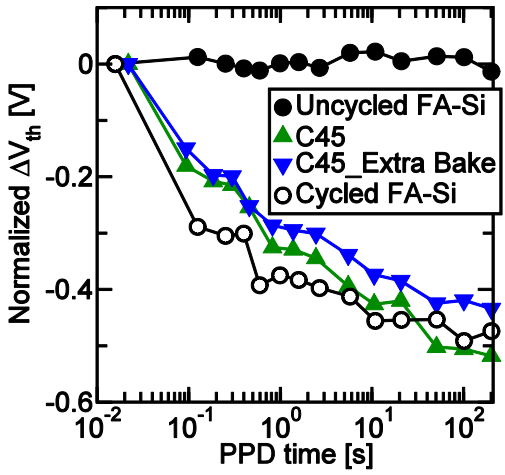


Figure 4.42: Short-term retention by applying PPD measurements for FA-Si and $In_{0.45}Ga_{0.55}As$ channels with Cl_2-based cleaning (C45). On FA-Si channels, PPD is performed both on uncycled devices and on 100 *P/E* cycled devices.

4.6 Conclusions

Epitaxially grown $In_xGa_{1-x}As$ channel

The formation of the $In_xGa_{1-x}As$ channel as well as the filling capability and its composition, are investigated by exploring different Ga precursors (TEGa, TMGa), flow ratios and growth temperatures (in a range between 450 ˚C and 580 ˚C).

$In_xGa_{1-x}As$ channel with compositions x ranging between 0.25 and 0.9 can be achieved by changing the *In*/*Ga* gas flow ratio, the deposition temperature and the *Ga* precursors: TEGa decomposes at lower temperature as compared to TMGa, allowing to obtain channels with higher [*Ga*].

The $In_xGa_{1-x}As$ channel is a crystal and it is characterized by misfit and threading dislocations at interface with the Si-substrate, due to the large lattice mismatch between Si and III-V. Planar defects (stacking faults, nanotwins) are also observed along the channel, probably due to an

unoptimized III-V nucleation on the Si starting surface or an insufficient surface preparation.

The channel filling capability increases with the growth temperature and larger channel diameters. However, for high deposition temperature (e.g., 580 ˚C) parasitic nucleation on oxide areas and premature closure of the memory hole are observed as a consequence of a growth rate increase with the temperature.

The channel lengths are variable, as already observed on $Si_{1-x}Ge_x$, probably due to process variations: roughness in the memory hole and on the top surface might induce un-balanced material diffusion/transport, while different starting surfaces introduce nucleation delays.

Metal drain and contact formation

The formation of source and drain junctions in Si-reference flow require a thermal budget as high as 1050 ˚C which is incompatible with $In_xGa_{1-x}As$. To cope with the lower III-V thermal budget, the source junction diffusion is skipped and Ti/TiN stack is used as drain instead of poly-Si drain.

The metal drain patterning is not straightforward. During the metal etch, residues are sputtered on the metal and on the exposed area (e.g., TSG). Sputtered residues compromise the quality of the final drain contact. Furthermore, they act as a mask, impeding a proper etch of the layers underneath (e.g., TSG, CG, BSG), and hence of the gates contacts. To overcome these issues, a tuning of the metal etching process and dedicated cleanings are required and developed.

Electrical performance

Among all the explored channel splits, $In_xGa_{1-x}As$ channels with x ranging between 0.25 and 0.55, are selected for the electrical characterization: TMGa is preferred over the TEGa, since it is the most used *Ga* precursor and the preferred growth temperature is 550 ˚C, based on the promising results obtained.

Different populations of devices are observed, resulting in different levels of I_{on} and I_{off}. In order to correlate the device operation with the III-V channel morphology/composition, TEM and EDS analysis are carried out. The obtained results indicate that the integration of the III-V channels is not fully optimized and the channels variability has a strong impact on the electrical performance: composition variability along the channel and the presence of *In* clusters are the cause of low or un-modulated current. On the other hand, devices which show modulated and high current are

characterized by a constant composition along the entire memory hole; these devices are selected for further electrical characterization.

The $In_xGa_{1-x}As$ performance improve by increasing [*In*], but at the expense of I_{off}: The [*In*] increase results in a reduction of the band gap, leading to higher mobility, and hence higher I_{on}. At the same time, lower band gaps facilitate the BTBT mechanism responsible for I_{off} increase. There are also other factors that can cause an I_{off} increase such as: TAT mechanisms due to the presence of defects at the channel/TuOx interface as well as possible Si diffusion into the channel. Si diffusion is expected to occur from the substrate during the $In_xGa_{1-x}As$ growth and acts as n-type dopant. The presence of dopants into the channel has also an impact on I_{on}.

$In_{0.45}Ga_{0.55}As$ channels have superior conduction properties compared to poly-Si channels, showing higher I_{on} and g_m and ~15 times higher mobility. However, the I_D-V_G curves are always characterized by a strong flattening, which in turn leads to an underestimation of the real III-V conduction characteristics. To better investigate the conduction properties of the III-V and FA-Si channels Scalpel SPM technique is used. This technique allows a direct access to the channel material and reveals that $In_xGa_{1-x}As$ channel conductivity is increased by a factor 1000 with respect to the one of poly-Si.

Surface preparation and memory performance

An in-depth analysis is conducted on the surface preparation required to initiate the III-V growth. The surface preparation is a critical step, as it must also guarantee the integrity of the TuOx, which is a crucial part of the memory stack.

Two alternative cleaning routes, namely HCl and Cl_2, are investigated and their impact on the TuOx and the memory performance are assessed.

HCl cleaning is conducted in H_2 ambient at temperatures ranging between 650 °C and 900 °C: it turns to be effective only at 900 °C, but at such high temperature the TuOx thickness is reduced, as already observed in epi-$Si_{1-x}Ge_x$ process flow. As a consequence, faster P/E characteristics and a retention loss of ~1 V after one day are observed. As the amount of consumed TuOx is difficult to control, HCl-based surface preparation is not suitable for future integration.

Thanks to the lower thermal budget involved, the Cl_2 route is able to preserve the TuOx thickness. This result is proven by the slow P/E performance caused by the thicker TuOx deposited preventively to compensate for possible consumption. Despite the thicker TuOx, the retention characteristic is not optimal: a significant charge loss, comparable

to the one of FA-Si devices with a degraded TuOx after 100 *P/E* cycles, is observed. The presence of near-interface TuOx defects may be caused by the III-V integration (e.g., surface preparation, III-V/TuOx incompatibility) as well as by the fact that the III-V integration flow does not have dedicated passivation steps. By introducing a bake at 625 °C in H_2 after the channel formation, the charge loss can be mitigated, thanks to a reduction of the TuOx defects.

Chapter 5

Advanced characterization

5.1 Introduction

This chapter focuses on the advanced characterization of the III-V devices presented in Chapter 4, the integration of optimized drain contact as well as the implementation of passivation steps.

The impact of the asymmetrical junctions on the electrical performance is investigated via the analysis of I_D-V_G and I_D-V_D characteristics performed by biasing either the source or the drain. Furthermore, TEM and EDS inspections are conducted, to correlate the electrical results (e. g. current flattening and asymmetrical behavior) with the morphology and the composition of both the channel and of the source/drain contacts.

TCAD simulations are carried out to better assess the asymmetrical current behavior as well as the strong saturation present in the I_D-V_G characteristics and to provide a guideline to improve the III-V devices.

Based on the results obtained by simulations, optimized III-V devices are proposed and integrated and benchmarked against epi-Si channel.

Finally, deuterium annealing is introduced to try to passivate the III-V channel/TuOx interface and to improve the defective TuOx, as observed in (4.5.2).

5.2 Asymmetrical junction study

As described in (4.3.3), III-V devices present asymmetrical junctions; the n^+ Si substrate serves as source junction, while a metal stack (Ti/TiN) is used as a drain to cope with the low thermal budget of the III-V compounds. In order to study the impact of the asymmetrical junctions on the electrical performance, I_D-V_G and I_D-V_D measurements are conducted.

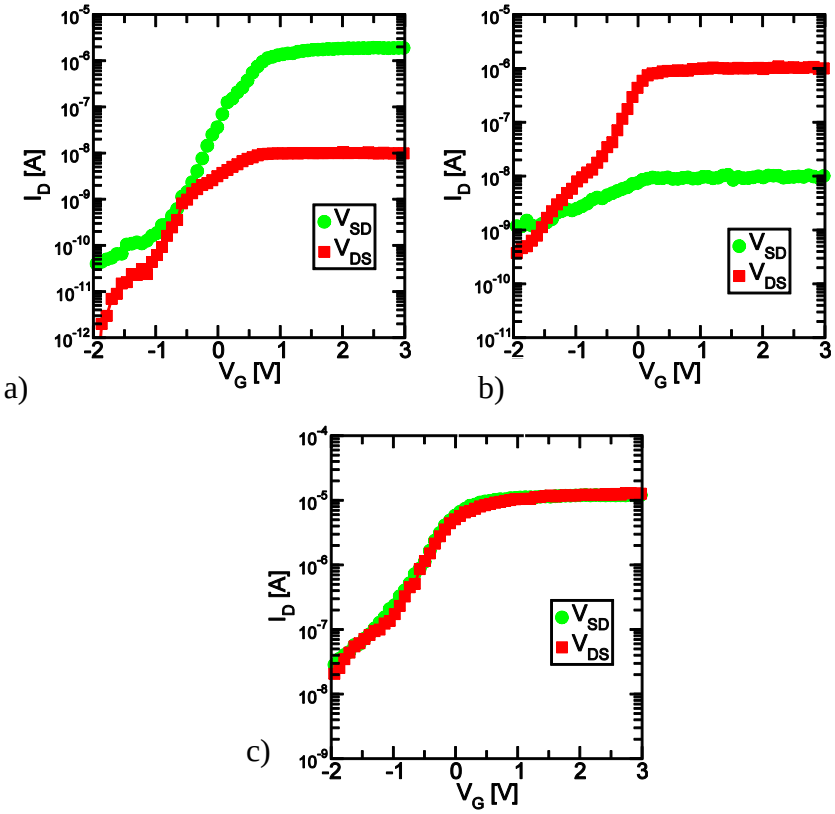


Figure 5.1: I_D-V_G are performed on ~70 devices. by sweeping the CG and by applying a drain-to-source (V_{DS}) or a source-to-drain bias (V_{SD}) of 0.5 V, while keeping the side gates at 5 V. On the wafer under investigation the devices show a) source dominance (~40% of the devices measured), b) drain dominance (~40%), c) same behavior independently of V_{DS} or V_{SD} (~20%). The percentage of devices showing a certain behavior can change from wafer to wafer.

In Fig. 5.1 different I_D-V_G characteristics are shown: in some cases the currents are asymmetrical, with a source or a drain dominance (Fig. 5.1.a and Fig. 5.1.b). In other cases there is an overlap of the curves, independently of V_{DS} or V_{SD} (Fig. 5.1.c). Despite their different behavior, all the I_D-V_G always feature a flattening for V_G > 1 V.

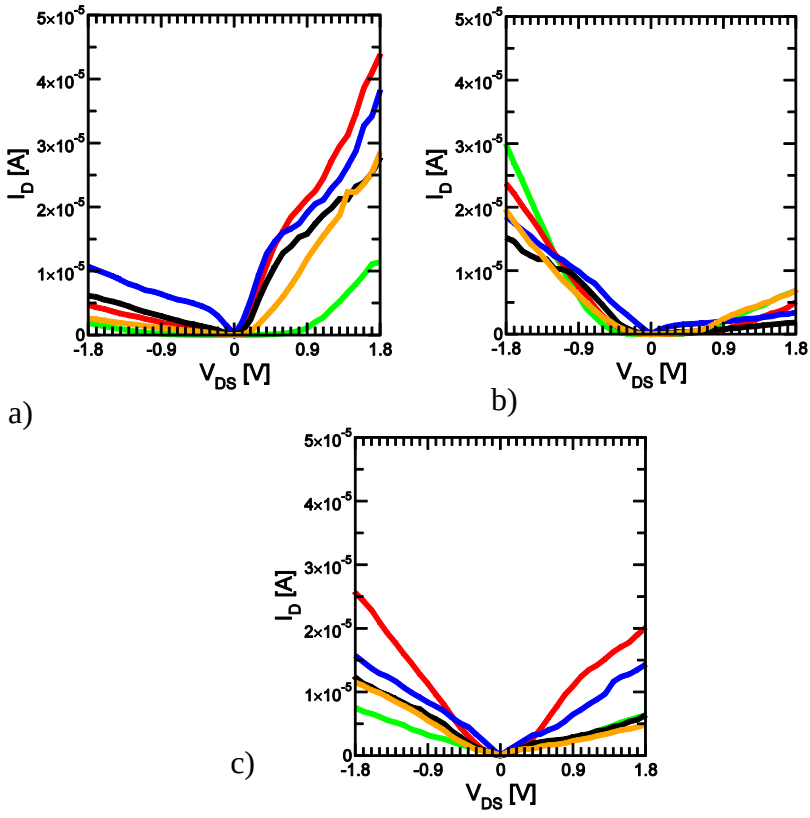


Figure 5.2: I_D-V_D measurements are performed by sweeping the drain (0 V< V_{DS} < 1.8 V) or the source (-1.8 V< V_{DS} < 0 V), while keeping all the 3 gates in pass mode (5 V). Devices are not always perfect resistors and they can show: a) source dominance, b) drain dominance, c) symmetric behavior.

The I_D-V_D characteristics, reported in Fig. 5.2, show high variability: curves are typically asymmetrical with a drain or source dominance

(Fig. 5.2.a and Fig. 5.2.b) and they are not always perfect resistors, but they can behave like a series of resistors or even diodes.

To clarify the cause of the different electrical behaviors, TEM inspections are conducted on a total of 8 devices coming from the different populations. Two morphologically different channels are observed, as shown in Fig. 5.3: there are undergrown channels (Fig. 5.3.a), which always present a drain dominance (higher current for V_{DS}) and overgrown channels (Fig. 5.3.b and 5.3.c), that can have either symmetrical I_D-V_G or source dominance (higher current for V_{SD}).

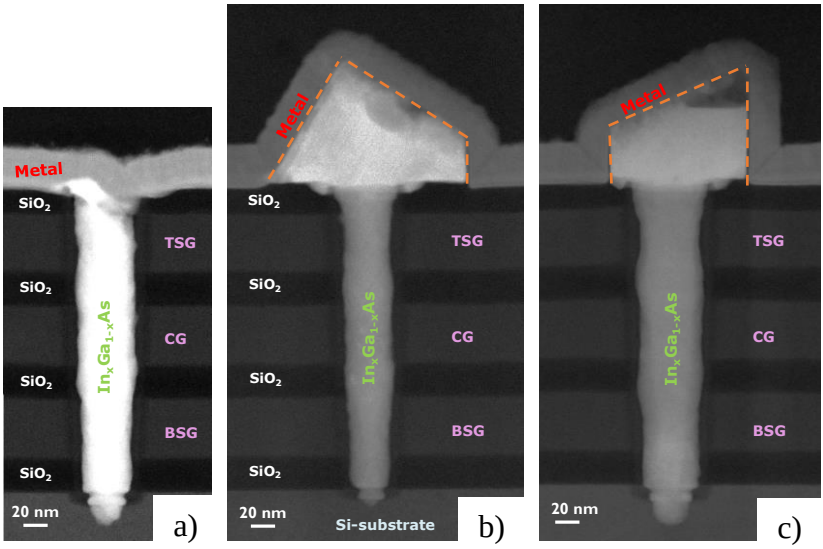


Figure 5.3: HAADF-STEM of III-V channels which show I_D-V_G with a) drain dominance, b) source dominance, c) symmetrical behavior.

The EDS analysis conducted on the STEM inspections reveals that the [*In*] is not always constant, independently of the channel length (Fig. 5.4). The [*In*] is always lower close to the Si-source. Instead, a drift of [*In*] is observed close to the metal drain and it seems to be correlated to the I_D symmetry: the [*In*] decreases on devices with drain dominance (Fig.5.4.a), while it increases on devices with source dominance (Fig.5.4.b). Devices which have a symmetrical current present constant [*In*] (Fig. 5.4.c).

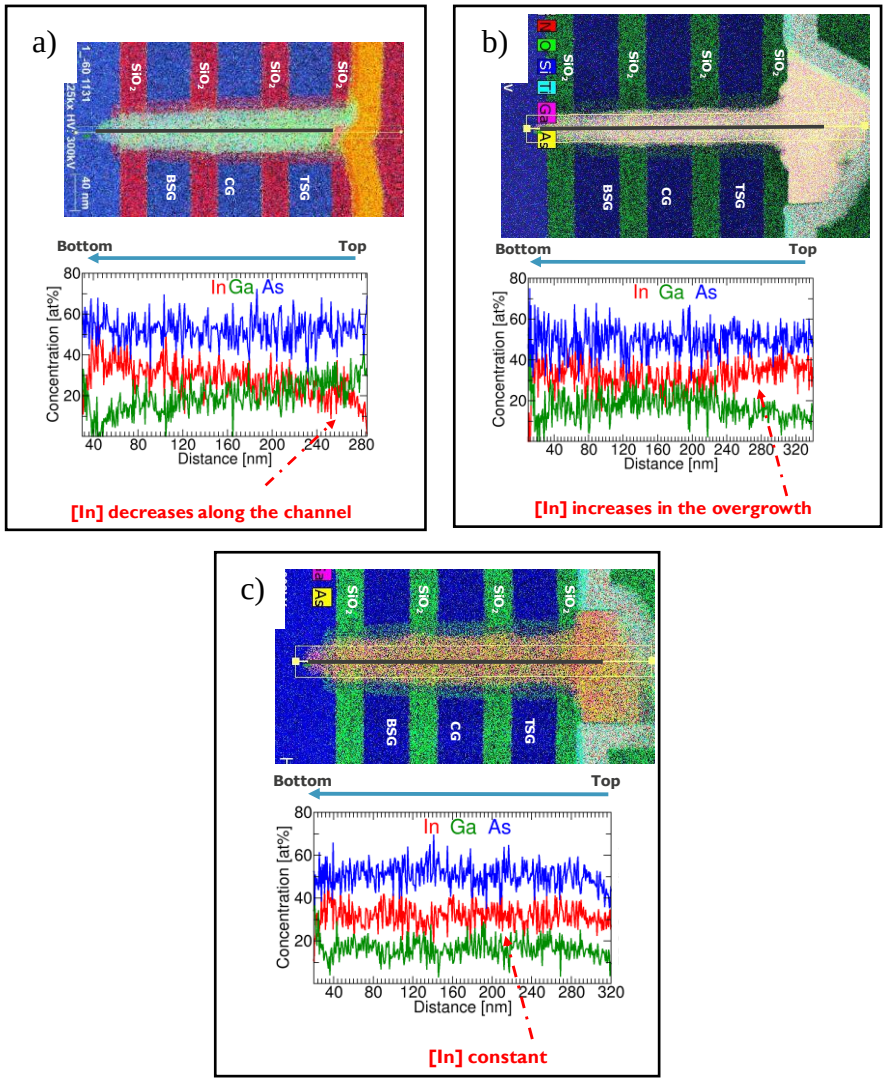


Figure 5.4: EDS mapping of devices a) with drain dominance show lower [*In*] at the drain side, b) with source dominance are characterized by higher [*In*] close to the drain, c) with symmetrical behavior have constant [*In*].

Furthermore, the devices with drain dominance (undergrown ones) always present inhomogeneous composition at the metal drain side, as reported in Fig. 5.5.b; *In*-rich or *Ga*-rich islands are observed, as well as GaAs and Ti-As regions (Fig. 5.5.c). The mixture of Ti-As (or Ti-Ga) is a typical

product of the contact between $In_xGa_{1-x}As$ and *Ti*, as reported in [160], and compromises the drain quality.

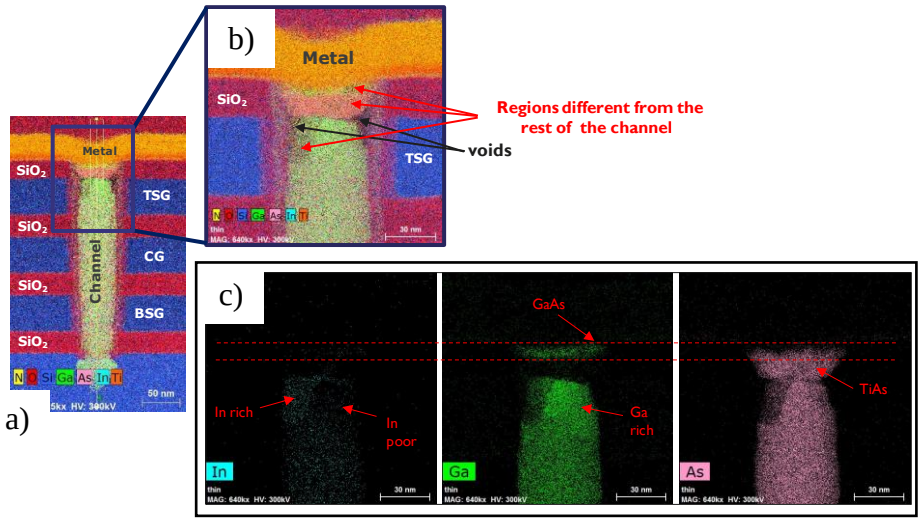


Figure 5.5: a) EDS map on a III-V channel with a drain dominance (higher current for V_{DS}). b) Zoom-in of the upper part of the channel; voids and inhomogeneous composition are detected. c) EDS map highlighting In, Ga, As elements of the channel close to the metal drain.

5.3 Sentaurus Simulations

Device simulations are carried out to qualitatively understand the impact of composition and channel morphology variabilities on the electrical performance and to find a pathway for the device improvement.

2-D simulations are performed in cylindrical geometry by using Synopsys Sentaurus Device [161]. The simulated structure, sketched in Fig. 5.6.a, mimics "SAKKARA", imec's 3-D NAND test vehicle (Fig. 5.6.b), and features a vertical symmetry axis to take into account the cylindrical geometry.

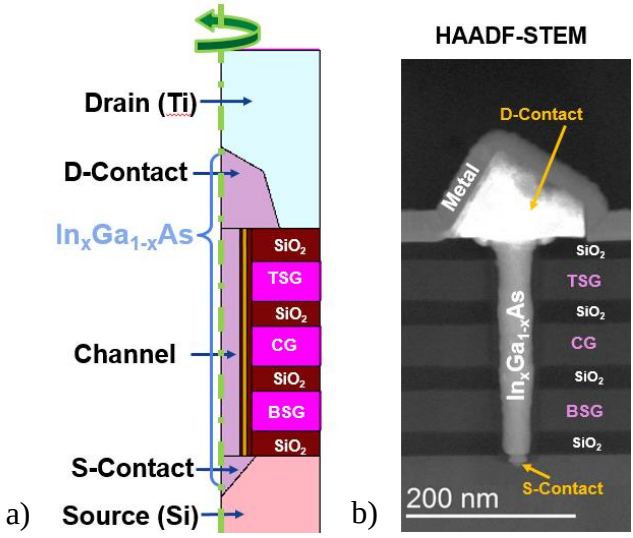


Figure 5.6: a) Structure used for simulation mimicking "SAKKARA" test vehicle. b) HAADF-STEM of the III-V channel to be simulated.

5.3.1 Simulations Setup

Sentaurus device numerically solves Poisson for the carrier density and the electric field and the drift-diffusion model for the currents on a meshed finite element structure representing the device under investigation. Furthermore, it includes Fermi-Dirac statistics for the energetic distributions of the carriers. The mobility model is given by the physical parameters of the simulated material, and hence by its stoichiometry. In addition, the mechanisms associated to the presence of defects (e.g., Shockley-Read-Hall, TAT, Fermi-level pinning [148], [152]-[154]), or associated to the narrow band gap (e.g., BTBT [148]), can be simulated in Sentaurus by using phenomenological models which require a wide number of fitting parameters. Since these values are un-known, the qualitative investigation might become completely fictitious. Therefore, the simulations are limited to the pure electrostatics, which do not require any fitting parameters. Simulations require that the channel is slightly doped. Moreover, in (4.4.3) it has already been mentioned that the III-V channel might be characterized by impurities such as Si diffusion from the substrate that acts as n-type dopant [149].

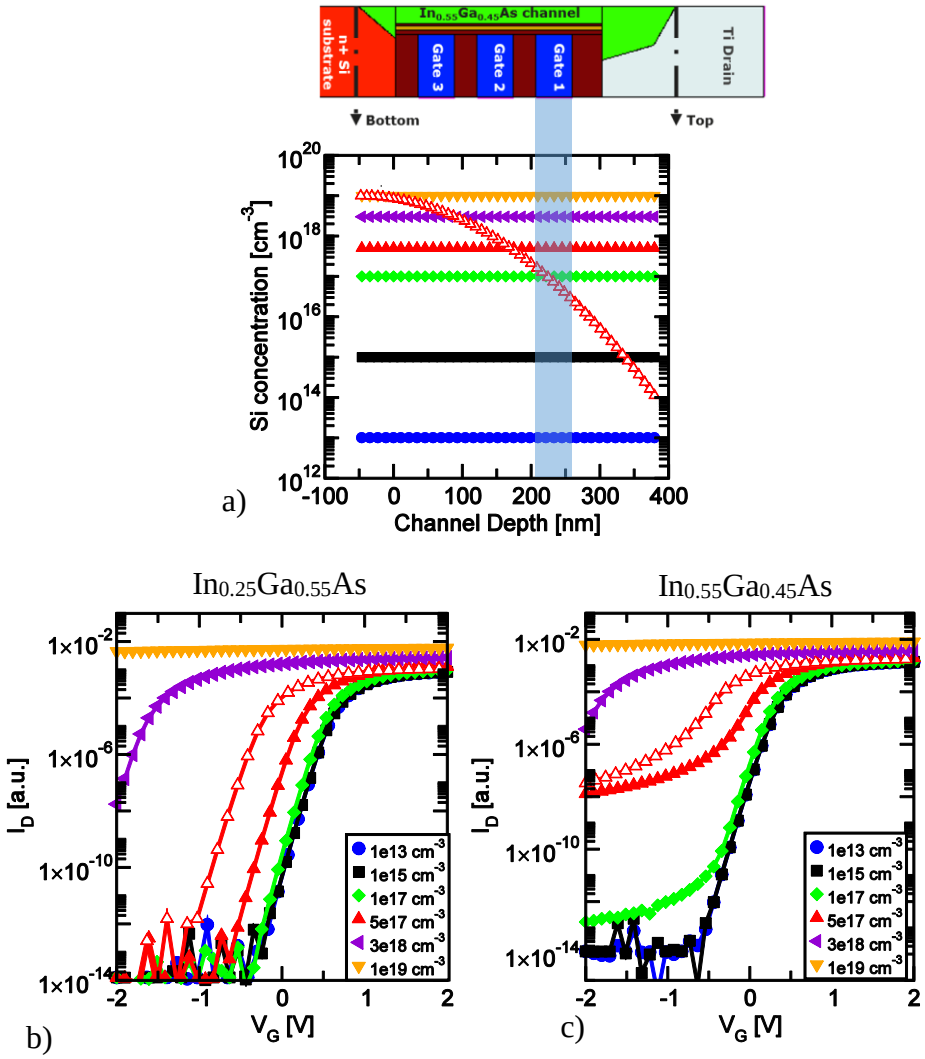


Figure 5.7: a): Simulated Si profiles as a function of the channel depth; the uniform profiles are reported with solid symbols while the non-uniform one is reported with open symbols. I_D-V_G characteristics by sweeping the CG, for b) $In_{0.25}Ga_{0.75}As$ channels, and c) $In_{0.55}Ga_{0.45}As$ channels as a function of different [*Si*] and doping profiles.

The quantification of possible *Si* diffusion is not straightforward, as its concentration is too low to be assessed by spectroscopic analysis (e.g., EDS)

and the dimension of the devices prevents the use of more sensitive techniques (e.g., TOF-SIMS), as they could be influenced by the *Si* which surrounds the III-V channel. Therefore, to achieve results which are as close as possible to the measurements, different profiles and n-type doping concentrations are simulated on $In_xGa_{1-x}As$ channels, with x equals to 0.25 and 0.55, respectively, as shown in Fig. 5.7: low I_{off} is observed in channels with a doping concentration lower than $1x10^{17}$ cm^{-3}, independently of the [In]. As the doping increases, the I_D-V_G shifts towards negative V_G values. When a doping in the range of $0.5x10^{18}$-$1x10^{18}$ cm^{-3} close to the CG is used in conjunction with a smaller band gap material ($In_{0.55}Ga_{0.45}As$), a significant increase of I_{off} (6 orders of magnitude) is shown. Instead, larger doping (e.g., $3x10^{18}$ cm^{-3}) impedes the devices from being turned off, irrespectively of [*In*].

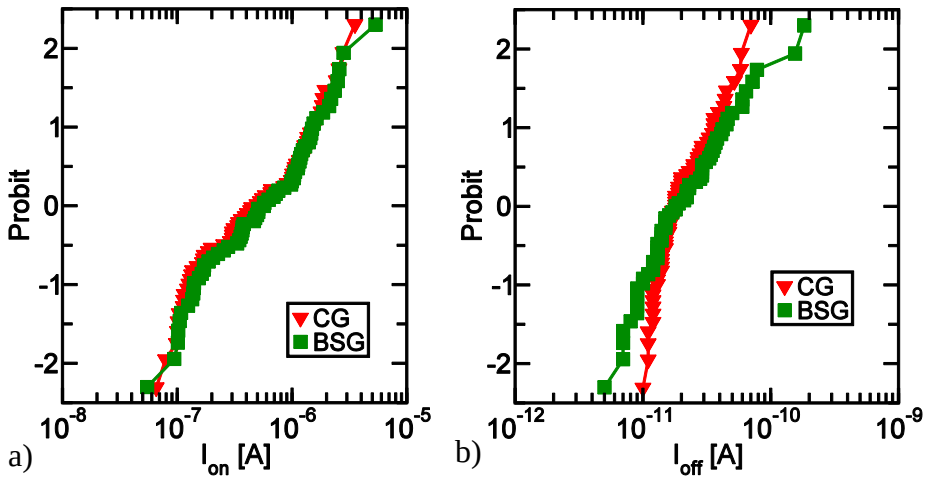


Figure 5.8: Distribution of a) I_{on} at fixed V_{ov} (2 V) and b) I_{off}, by sweeping either the CG or the BSG (from -2 V to 4 V) on $In_{0.25}Ga_{0.75}As$ channels. Similar distributions are observed, suggesting that the doping in the CG and BSG transistors is uniform.

The measured I_{off} data, reported in (4.4.3), can be qualitatively reproduced by simulations (Fig. 5.7) if the dopant present in the CG transistor has a concentration in the range of $0.5x10^{18}$-$1x10^{18}$ cm^{-3}; this is valid for both uniform and non-uniform profiles, provided that the dopant in the CG transistor is in the same order. However, by using the non-uniform profile, the dopant next to the BSG (the transistor close to the substrate) is

high enough to have un-modulated current, contrary to the measured results shown in Fig. 5.8: the distributions of the I_{on} and I_{off} by sweeping either the BSG or the CG on $In_{0.75}Ga_{0.25}As$ channels are comparable, indicating a quite uniform *Si* doping profile. Similar behavior is also observed in $In_{0.55}Ga_{0.45}As$ channels (not shown). Therefore, an uniform *Si* profile along the channel with a concentration of $5x10^{17}cm^{-3}$ is more compatible with the experimental data and it is chosen for further simulations.

5.3.2 Study of the current variability and saturation

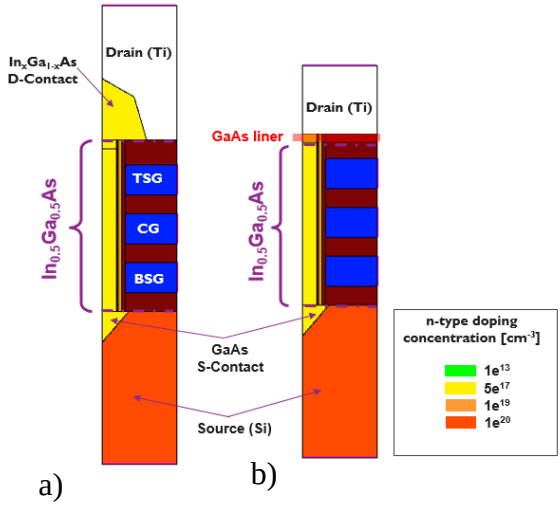


Figure 5.9: Sketches of the simulated structures mimicking a) overgrown and b) undergrown channels which are uniformly doped. GaAs in contact with *Ti* is added in undergrown channels to reproduce the EDS mapping in Fig. 5.5.

Figure 5.9 reports the sketches of the structures simulated for the assessment of the current variability and flattening observed in our devices (Fig. 5.2); the used structures mimic both overgrown (Fig. 5.9.a) and undergrown channels (Fig. 5.9.b), as shown by TEMs in Fig. 5.3. $In_{0.5}Ga_{0.5}As$ is used as channel material. To emulate the [*In*] gradient close to the junctions, as evidenced by TEM-EDS mapping (Fig. 5.4 and Fig. 5.5), InAs, $In_{0.5}Ga_{0.5}As$ and GaAs are used as D-Contact on the overgrown

portion of the channel (5.9.a). GaAs is always simulated as S-Contact and it is also used as D-Contact on undergrown channels (5.9.b).

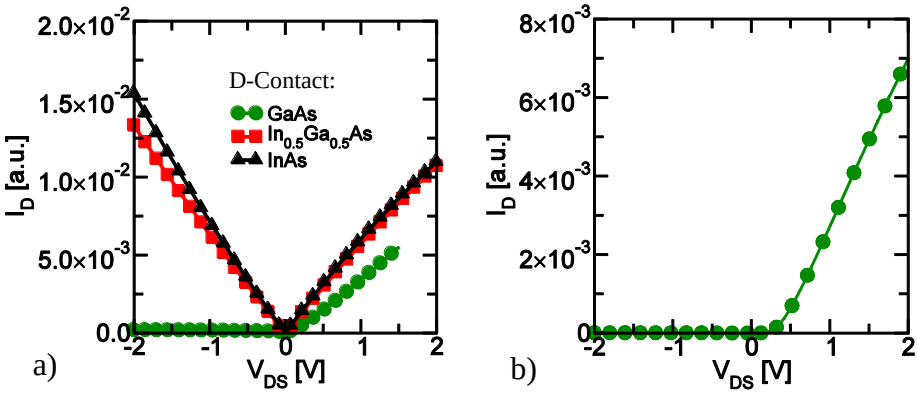


Figure 5.10: Simulated I_D-V_{DS} characteristics of a) overgrown channels by changing the [In] at the D-Contact and b) undergrown channels with GaAs in contact with the Ti drain; rectifying behavior is observed when GaAs is in contact with Ti.

I_D-V_{DS} simulations are conducted on the structures of Fig. 5.9 by sweeping the drain or the source from 0V up to 2V, while keeping all the gates in pass mode (5V).

In agreement with the measured data (Fig. 5.2.a, Fig. 5.5), simulations always show rectifying behavior with drain dominance when GaAs is in contact with Ti (Fig. 5.10.a-b). The rectifying behavior is caused by the fact that the GaAs electron affinity ($q\chi_S$ = 4.07 eV [103]) is lower than the Ti work function ($q\Phi_M$ = 4.33 eV [162]); at equilibrium a depleted region is present at GaAs/Ti interface and consequently a potential barrier (Φ_B) is formed (Fig. 5.11.a), leading to a Schottky contact [111].

I_D-V_{DS} characteristics close to the symmetrical case are observed on overgrown devices with $In_{0.5}Ga_{0.5}As$ or InAs as D-Contacts (Fig. 5.10.a); since the $q\chi_S$ of $In_{0.5}Ga_{0.5}As$ (4.48 eV [103]) and InAs (4.9 eV [103]) are larger than the $q\Phi_M$ of *Ti*, at equilibrium no Φ_B is present (Fig. 5.11.b) and electrons can flow freely through the III-V/Ti system, generating an ohmic contact [111]. However, simulations are not able to explain the rectifying behavior between the III-V and the *Si* source (Fig. 5.2.b); ideally III-V in contact with *Si*, should lead to an ohmic contact, as also demonstrated by simulations. In the real devices the lattice mismatch between III-V

compounds and Si causes interface defects and dislocations, as shown in the HR-TEM image of Fig. 4.14. The defective nature of the interface (which is not simulated) between Si and III-V could often lead to the formation of Schottky-contacts where ohmic ones would be expected [163].

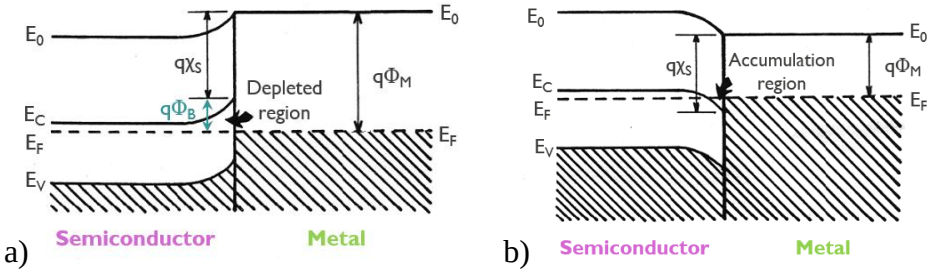


Figure 5.11: Band diagram for a n-type semiconductor-metal system with a) $q\chi_S$ larger than $q\Phi_M$ and b) $q\chi_S$ smaller than $q\Phi_M$; the first case results in the formation of a Schottky contact, while the second one generates an ohmic contact.

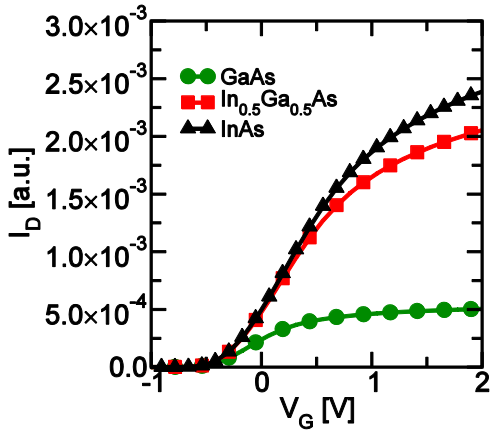


Figure 5.12: Simulated I_D-V_G characteristics of overgrown $In_{0.5}Ga_{0.5}As$ channels by changing the [*In*] at the D-Contact. The current flattening can be reduced by increasing the [*In*].

I_D-V_G curves are simulated on the structures sketched in Fig. 5.9.a by sweeping the CG, while keeping the side gates in pass mode (5V) and the drain at 0.5 V. Simulations are able to qualitatively reproduce the current

saturation when unfavorable material combinations (e.g., GaAs in contact with *Ti*) are present at the drain side, as reported in Fig. 5.12; this result indicates that the current flattening is caused by a high series resistance introduced outside of the channel (e.g., the drain).

5.3.3 Pathway for device improvement

Simulations offer a guideline to improve the III-V devices. First, the doping into the channel has to be limited as much as possible, to reduce the I_{off}, as observed in the simulations reported in Fig. 5.7. Highly doped S/D-Contacts must be used to guarantee an ohmic contact and to reduce the source/drain series resistance [164]. Based on these elements, the structure suggested to achieve better performance is sketched in Fig. 5.13.

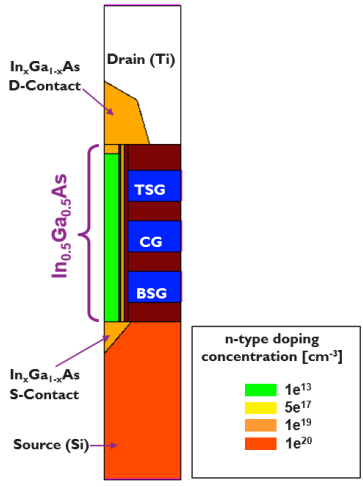


Figure 5.13: Sketch of the simulated structures suggested for the III-V device improvement. Channel has to be un-doped, the S/D contacts must be highly doped.

To select the best material to be used as S/D-Contact, I_D-V_{DS} characteristics are simulated for the structures sketched in Fig. 5.13, by varying the $In_{1-x}Ga_xAs$ composition at the S-Contact or at the D-Contact.

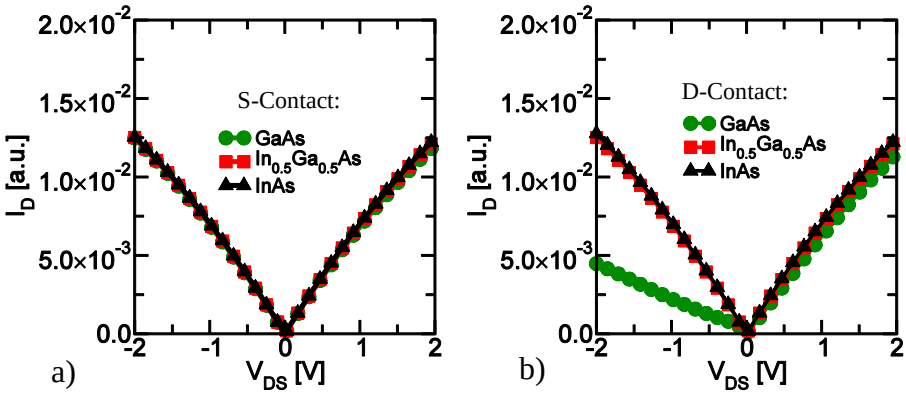


Figure 5.14: Simulated I_D-V_{DS} characteristics of overgrown $In_{0.5}Ga_{0.5}As$ channel with highly doped S/D contacts (Fig. 5.13) by changing the [*In*] at a) the S-Contact and b) at the D-Contact. Perfect overlap of the I_D-V_{DS} is always shown except when GaAs is used as D-Contact.

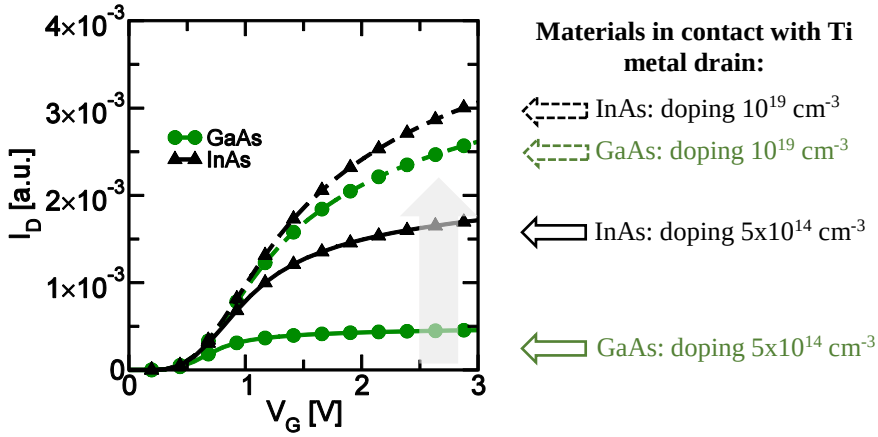


Figure 5.15: Simulated I_D-V_G characteristics of un-doped overgrown $In_{0.5}Ga_{0.5}As$ channels by changing the [*In*] and the doping level at the D-Contact. A reduction of the current saturation is achieved by choosing the proper material and doping configuration at the drain side.

According to simulations, an ohmic contact can be obtained independently of the [In] at the S-Contact, provided that it is doped, as indicated by the perfect overlap of the symmetrical I_D-V_{DS} curves in

Fig. 5.14.a. On the other hand, GaAs used as D-Contact is not able to restore the symmetrical I_D-V_{DS}, as for the case of $In_{0.5}Ga_{0.5}As$ and InAs (Fig. 5.14.b). The doping level in the GaAs D-Contact is not sufficient to reduce the Φ_B between the Ti and the semiconductor (Fig. 5.11.b). Therefore to avoid a Schottky contact formation, $In_xGa_{1-x}As$ with high [In] is preferred as D-Contact. High [In] helps to lower the Schottky Φ_B between the D-Contact and the metal drain. This leads to a reduction of the drain resistance [164], and hence of the current flattening, as shown in Fig. 5.15; the drain resistance can be further mitigated by increasing the D-Contact doping level.

5.4 Integration of optimized D-Contact

The III-V process integration flow, described in (4.3), is slightly modified in order to optimize the D-Contact, as suggested by simulations conducted in the previous section. To assess the D-Contact optimization, partitioning tests are conducted, as sketched in Fig. 5.16.

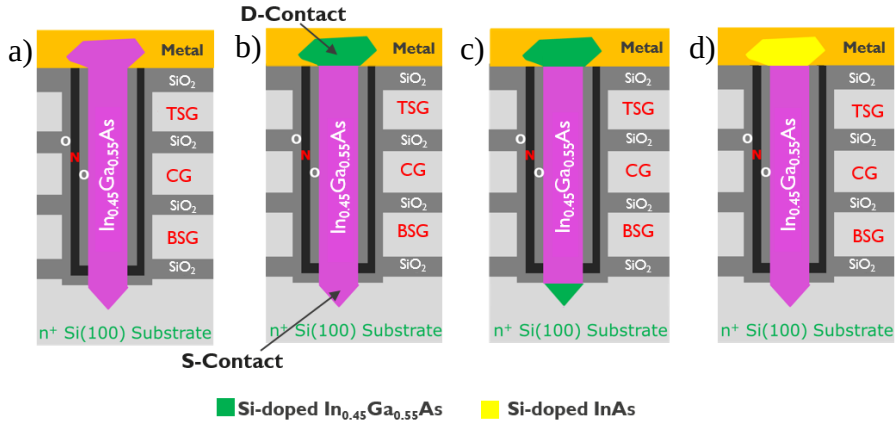


Figure 5.16: Sketches of a) un-optimized epi-$In_{0.45}Ga_{0.55}As$ channel, b) optimized D-Contact with Si-doped $In_{0.45}Ga_{0.55}As$, c) optimized S/D-Contact with Si-doped $In_{0.45}Ga_{0.55}As$ and d) optimized D-Contact with Si-doped InAs.

As for the case of epi-$Si_{1-x}Ge_x$ in "STRATO" test vehicle (3.3), a time-based approach is used for the fabrication of the optimized devices: the integration is conducted in three in-situ subsequent steps. First, Cl_2 route is used for the surface preparation, as described in (4.3.1). Then, $In_{0.45}Ga_{0.55}As$ is grown to form the channel; the growth time (t_{growth}) can vary, as summarized in Table 5.1. Next, the epi-growth is switched either to *Si*-doped $In_{0.45}Ga_{0.55}As$ (recipes A and B in Table 5.1) or to *Si*-doped InAs (recipes C and D in Table 5.1), to create the D-Contact. Silane (SiH_4) is added during the growth, to intentionally dope the D-Contact. An attempt to improve the S-Contact is also done and consists in starting the growth with Si-doped $In_{0.45}Ga_{0.55}As$ (recipe B in the Table 5.1) and continuing with the channel and the drain formation, as described above.

Recipe Name	S-Contact	Channel	D-Contact
C45	$In_{0.45}Ga_{0.55}As$		
	(t_{growth}: 1000s)		
A	$In_{0.45}Ga_{0.55}As$		Si-doped $In_{0.45}Ga_{0.55}As$
	(t_{growth}: 700s)		(t_{growth}: 300s)
B	Si-doped $In_{0.45}Ga_{0.55}As$	$In_{0.45}Ga_{0.55}As$	Si-doped $In_{0.45}Ga_{0.55}As$
	(t_{growth}: 100s)	(t_{growth}: 600s)	(t_{growth}: 300s)
C	$In_{0.45}Ga_{0.55}As$		Si-doped InAs
	(t_{growth}: 1000s)		(t_{growth}: 150s)
D	$In_{0.45}Ga_{0.55}As$		Si-doped InAs
	(t_{growth}: 700s)		(t_{growth}: 600s)

Table 5.1: Recipes description for the optimization of the S/D-Contacts for III-V devices (A-D); the integration of the optimized devices relies on a time-based approach. Recipe C45 represents the III-V reference with no S/D optimization. The deposition temperature is always kept at 550 ˚C.

5.4.1 Electrical characterization

I_D-V_G characteristics are collected on all the recipes summarized in Table 5.1, by sweeping the CG from -2 V up to 4 V, while keeping the side gate at 5 V and the drain at 0.5 V. Different device operation is observed,

due to the high channel variability (4.4.1), but the electrical analysis is conducted only taking into account devices with high current (see Table 4.3).

Fig. 5.17 compares the I_{on} and I_{off} distribution of the un-optimized III-V device (recipe C45 of Table 4.2) and of the devices with S/D-Contacts optimized by using Si-doped $In_{0.45}Ga_{0.55}As$ (recipes A and B in Table 5.1): independently of the S/D optimization, those devices show comparable I_{on} and I_{off} distributions. Most probably, the S-Contact is already highly doped, due to Si in diffusion from the substrate, so that the further doping in this region does not have any impact on the conduction. Furthermore, a t_{growth} of 300 sec may not be sufficient to create a doped D-Contact (see Table 5.1), needed to improve the current.

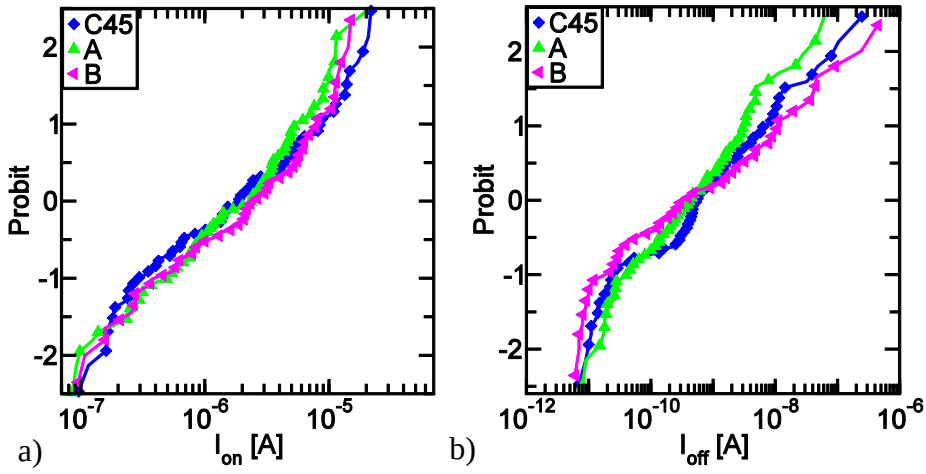


Figure 5.17: Distribution of: a) I_{on} at fixed V_{ov} = 2 V, and b) I_{off} of un-optimized devices (C45), and devices with D-Contact and S/D-Contacts optimized by using Si-doped $In_{0.45}Ga_{0.55}As$ (see Tab. 5.1). Independently of the S/D optimization, no significant current improvement is observed.

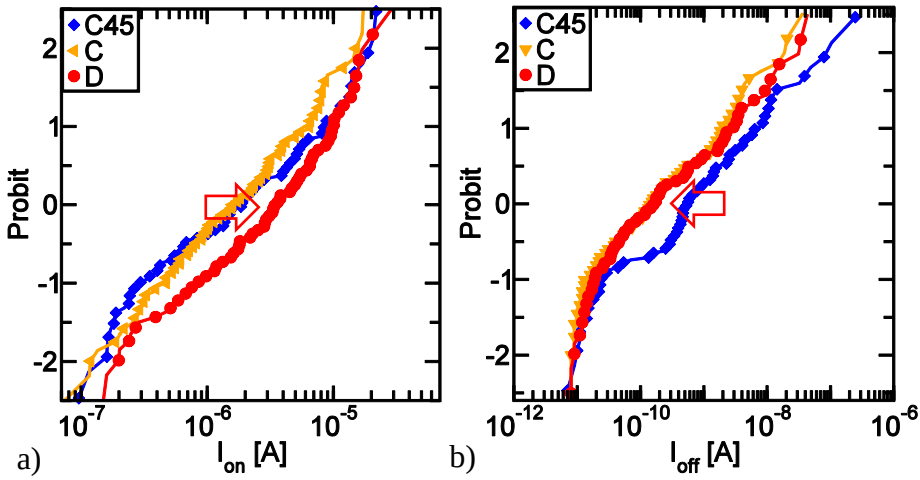


Figure 5.18: Distribution of: a) I_{on} at fixed V_{ov} = 2 V, and b) I_{on} of un-optimized devices (C45), and devices with D-Contact optimized by using Si-doped InAs with different t_{growth} (see Tab. 5.1); recipe D which shows improved I_{on}, has larger D-Contact.

The integration of recipe C (smaller Si-doped InAs as D-Contact and longer channel, as reported in Table 5.1) results in a slight I_{off} improvement without any impact on I_{on}, as compared to C45 (Fig. 5.18). On the other hand, if the channel t_{growth} is reduced and the Si-doped InAs D-Contact is made larger (recipe D in Table 5.1), a slight improvement of both I_{on} and I_{off} is observed (Fig. 5.18.a, Fig. 5.18.b). Given the fact that the channel is shorter, the D-Contact might be inside the memory hole. However, the reduced value of I_{off} (Fig. 5.18.b) excludes the presence of Si-doped InAs in the CG device. Therefore, the I_{on} enhancement can be attributed to the reduction of the drain resistance thanks to the highly doped D-Contact. In order to verify this aspect, in the next section a method for the extraction of the resistance introduced by the S/D contact is proposed.

5.4.2 R_{DS} extraction

The most commonly used technique for the extraction of the D/S series resistance (R_{DS}) is the so-called "L-array method", which requires I_D–V_G measurements over different channel lengths [165]–[167]. However, in the

literature other techniques, with different approximations and levels of accuracy, can also found: the R_{DS} can be extracted from the ratio of two I_D–V_G curves recorded at two different drain biases, with the assumption that the gate oxide capacitance (C_{ox}) , R_{DS}, L_{eff} and μ (defined in (4.4.2)) are constant at low V_{DS} (e.g., 10 and 50 mV) [168]. Alternatively, some R_{DS} extraction methods are based on sophisticated C–V measurements [169], while others rely on constant mobility criteria [170], which in any case require split C-V, as well as several fitting parameters.

As already discussed in (4.4.2) for the extraction of μ, we do not have any structures with different channel lengths, or dedicated structures for C-V measurements. Therefore, the R_{DS} extraction is just conducted from I_D-V_D curves in linear regime; first of all, the total device resistance (R_{tot}) is generalized as:

$$R_{tot} = \frac{V_{DS}}{I_{DS}} = R_{channel} + R_D + R_S = R_{channel} + R_{DS} \ , \qquad (5.1)$$

where $R_{channel}$ is the resistance of the entire string, which includes the three transistors channels together with the IGS regions, while R_{DS} is the external resistance introduced by the D/S contacts, as shown in the sketch of Fig. 5.19.

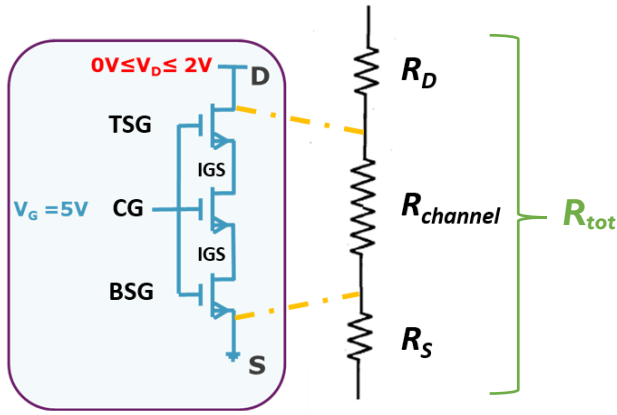


Figure 5.19: Sketch of the R_{tot} in our 3-D NAND string.

I_D-V_D characteristics are then performed by sweeping the drain from 0 V up to 2 V, with a step of 100 mV, while keeping all the gates in pass mode (5 V). For V_G equal to 5 V, I_D-V_G characteristics present a strong saturation, which starts already for lower V_G (~ 1V), as reported in Fig. 5.20; this result

indicates that the R_{DS} prevails over the $R_{channel}$: the gates are no longer able to control the channel conduction. Therefore, in this operation regime the R_{DS} can be assumed much larger than $R_{channel}$ and Eq. (5.1) can be approximated to:

$$R_{tot} = \frac{V_{DS}}{I_{DS}} \approx R_{DS} \tag{5.2}$$

The R_{DS} is extracted by using Eq. (5.2) after smoothening the I_D-V_D curves and is finally reported as the average of the resistances extracted for the whole range of applied V_{DS}.

Figure 5.21 shows the R_{DS} distributions of ~50 devices with un-optimized and optimized D-Contact; the median R_{DS} value of optimized devices is ~5 times lower than the one in un-optimized devices. Equation (5.2) does not allow to separate R_D and R_S. Nevertheless, since the only difference between both structures is in the D-Contact formation, it is possible to conclude that the R_{DS} reduction is related to the drain contact improvement.

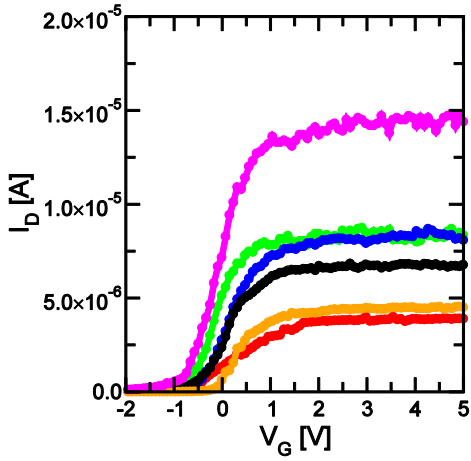


Figure 5.20: Typical I_D-V_G characteristics of III-V channels. The saturation of the curves is attributed to the R_{DS} dominance over the $R_{channel}$.

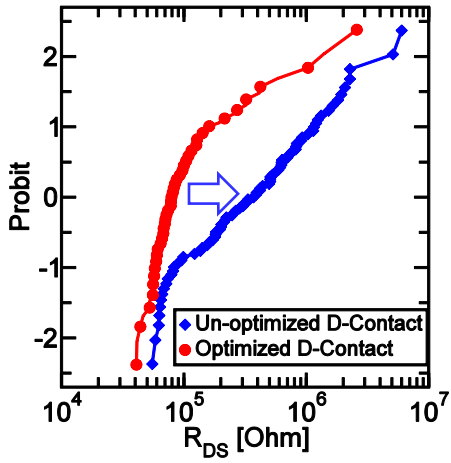


Figure 5.21: Statistical distribution of R_{DS} for un-optimized and optimized D-Contact (see recipes C45 and D in Tab. 5.1); the R_{DS} is reduced by using Si-doped InAs instead of un-doped $In_{0.45}Ga_{0.55}As$ as D-Contact.

5.4.3 Epi-Si channel integration as benchmark material

In Chapter 4 the electrical performance of III-V (epitaxially grown) have been compared with the ones of poly-Si channels. To have a better comparison, in this section epi-Si channel is used as benchmark material. Furthermore, ~4 nm thick PEALD TuOx is used in place of the HTO both in epi-Si and III-V devices, to investigate possible TuOx quality improvement.

The epi-Si integration is characterized by two in-situ subsequent steps: the surface preparation is done by using the Cl_2 route (4.3.1) and it is immediately followed by the epi-Si channel formation at 810 ˚C. Both the cleaning and the channel are done in a LPCVD system. The junctions formations follows as for the case of III-V (4.3.3). Contrary to the III-V process flow, a FGA is applied for 30 min and at 400 ˚C, after the entire wafer processing, to passivate the channel/TuOx interface.

Figure 5.22 benchmarks epi-Si against III-V channels: III-V devices show more widely distributed I_{on} (Fig. 5.22.a) and I_{off} (Fig. 5.22.b). The

median value of I_{on} does not significantly exceed the ones of epi-Si channels, while an improvement is observed above 1 σ, where III-Vs show ~7 times higher conduction, but with a penalty in I_{off} (Fig. 5.22.b). The low I_{off} value in epi-Si devices can be related to many factors such as: the larger Si band gap, which reduces the BTBT mechanism [148], [171], the fact that epi-Si channel is un-doped, the better channel/TuOx interface, as suggested by the *STS* in Fig. 5.23.

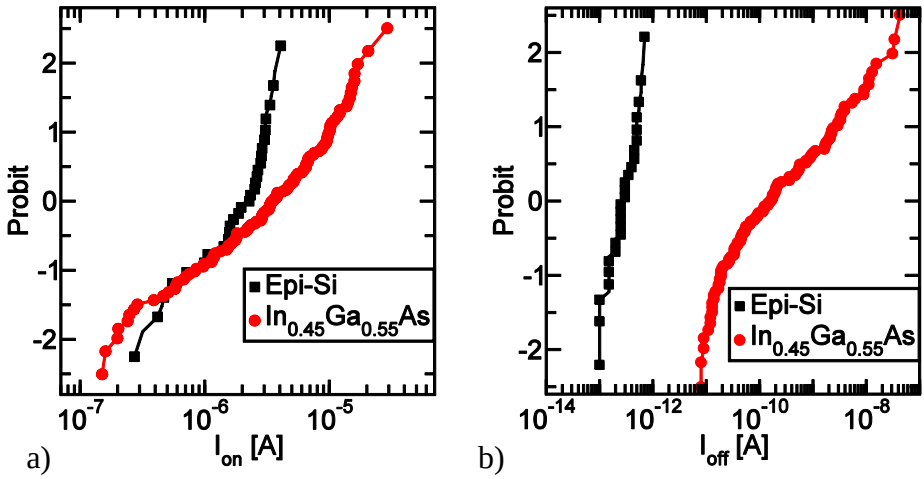


Figure 5.22: Distributions of a) I_{on} at fixed V_{ov} = 2 V and b) I_{off} for epi-Si, and $In_{0.45}Ga_{0.55}As$. III-Vs show wider distributions, improved I_{on} above 1 σ as well as a penalty in I_{off}.

The *STS* distribution of epi-Si appears to be bimodal (Fig. 5.23): a tightly distributed mode is centered around 0.1V/dec, similar to what is observed in epi-Si channels integrated in "STRATO" (3.6), while a more widely distributed mode ranges from 0.2 V/dec to 1 V/dec. The improved *STS* in epi-Si is the result of the better compatibility between Si and SiO_2 [172] and the interface passivation via FGA.

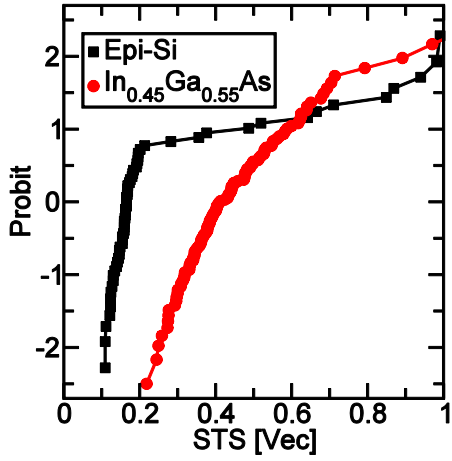


Figure 5.23: *STS* distributions for epi-Si, and $In_{0.45}Ga_{0.55}As$. Epi-Si shows better *STS*.

Memory performance are evaluated by performing *ISPP*/*ISPE* and long term retention measurements, as described in (4.5.1). The III-V devices have similar program and slower erase as compared to epi-Si (Fig. 5.24): the measured *P/E* characteristics are in contrast with the simulated ones shown in Fig.4.38.a, where slower program and faster erase have been reported for the III-V devices. These results indicates that the real band offsets are different from the values used in the simulations (Fig. 4.38.b): the electrons band heights between the systems III-V/TuOx and Si/TuOx are comparable, leading to similar program characteristics. Furthermore, since the III-V devices have smaller band gap, the holes band height in the III-V/TuOx becomes larger as compared to the Si/TuOx system, causing slower erase.

By comparing the long term retention characteristics, it is found that epi-Si presents less charge loss than the III-V devices (Fig. 5.25). This can be a consequence of a lower density of the near-interface TuOx defects, as demonstrated by PPD measurements, conducted as described in (4.5.2) and shown in Fig. 5.26: epi-Si devices do not have any ΔV_{th} shift for the whole PPD duration, indicating no defective TuOx. III-Vs instead, present a larger charge loss that can be, however, slightly reduced by using PEALD rather than HTO as TuOx.

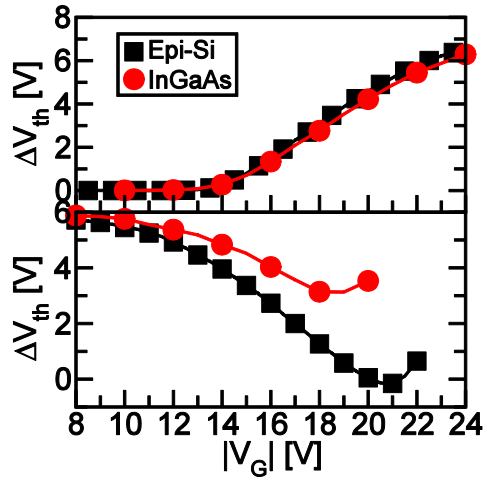


Figure 5.24: Measured *ISPP*/*ISPE* for $In_{0.45}Ga_{0.55}As$ and epi-Si channels. III-V devices show similar program and slower erase as compared to epi-Si; these results are in contrast with the simulated *ISPP*/*ISPE* shown in Fig. 4.38.a.

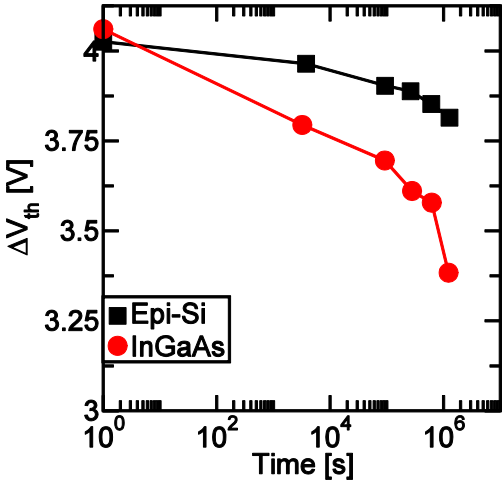


Figure 5.25: Long-term retention for Epi-Si and $In_{0.45}Ga_{0.55}As$ channels, with PEALD TuOx. III-V channels show a significant retention loss.

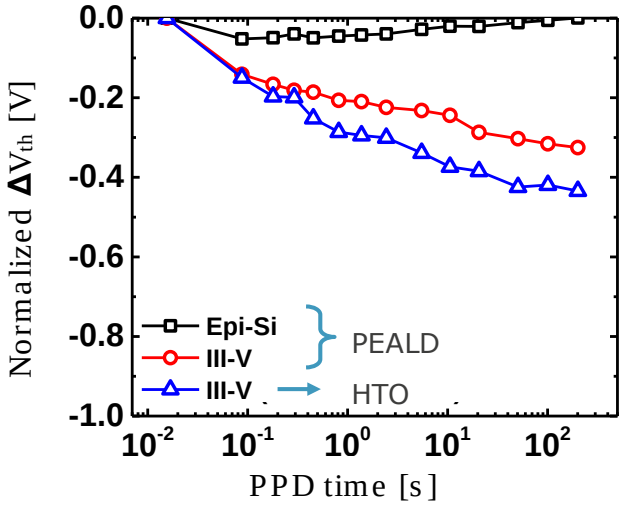


Figure 5.26: PPD measurements for Epi-Si with PEALD TuOx and $In_{0.45}Ga_{0.55}As$ channels with either PEALD or HTO as TuOx. III-V shows a larger charge loss as compared to Epi-Si, indicating higher density of near-interface TuOx defects. The charge loss can be partially mitigated by using PEALD in place of HTO TuOx.

The higher thermal budget involved during the epi-Si growth as well as the FGA, can help to cure the TuOx defects leading to an improved retention. Contrary to epi-Si devices, no passivation step is applied to the III-V case. In the next section, deuterium annealing will be used to investigate if it is possible to improve the III-V/TuOx interface, as well as the TuOx defectivity.

5.5 Deuterium annealing

Better conduction properties with a reduced *STS* and V_{th} have been observed in poly-Si reference devices by using high pressure (HP) deuterium (D_2) anneal rather than FGA or H_2 annealing [173]; these results are originated by a better passivation of the defects into the poly-Si channel and at interface with the TuOx [173].

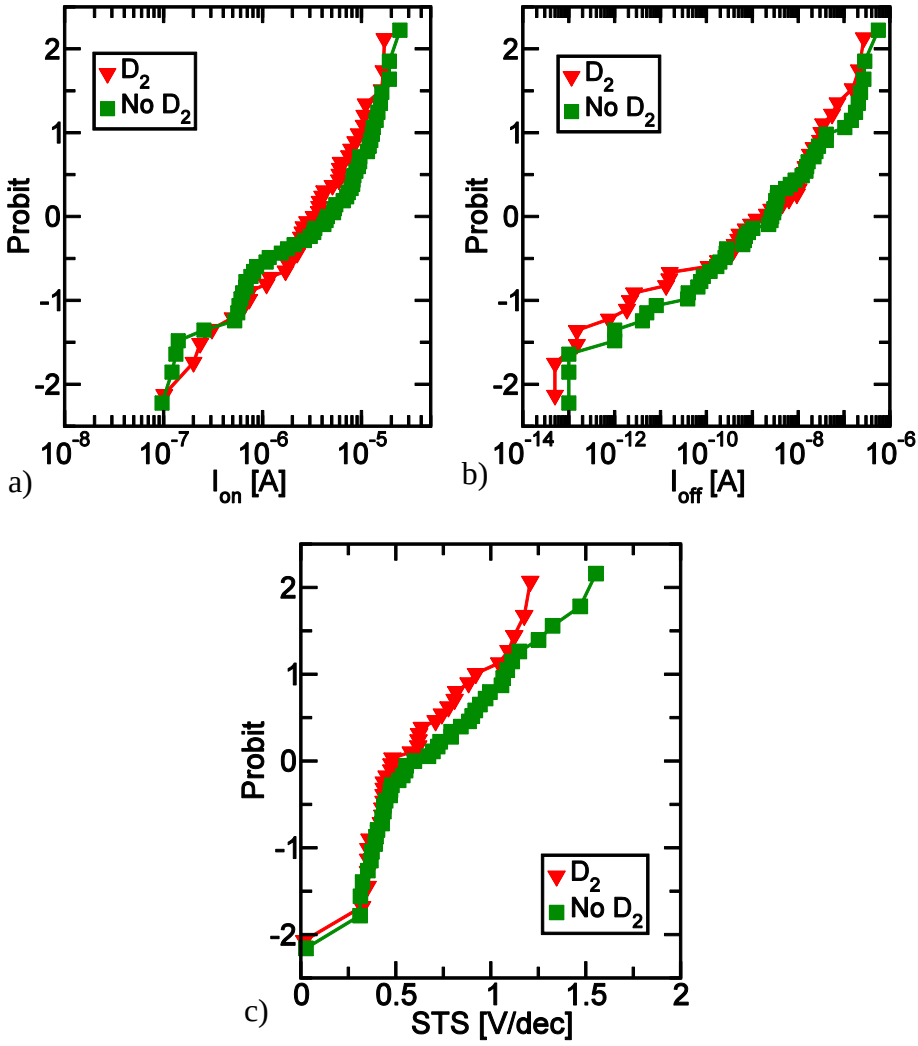


Figure 5.27: Distributions of a) I_{on} at V_{ov} of 2 V, b) I_{off} and c) *STS* for $In_{0.45}Ga_{0.55}As$ channels before and after D_2 annealing. An overlap of the curves is shown, indicating that D_2 annealing does not have much effect.

Based on the results reported in [173], HP-D_2 annealing is used on III-V devices. D_2 anneal is carried out after the full wafer processing at a pressure of 20 atm and at 400 ˚C for 30 min in a GENI SYS® system developed by Poongsan Corp. [174]; the annealing conditions are those used in [175].

Figure 5.27 shows the I_{on}, I_{off}, and *STS* distributions of the same set of $In_{0.45}Ga_{0.55}As$ devices measured before and after HP-D_2 anneal: an overlap

of the curves is observed. As evident from Fig. 5.28, no significant improvement is observed in long-term retention measurements. These results indicate that D_2 is not effective on our III-V devices

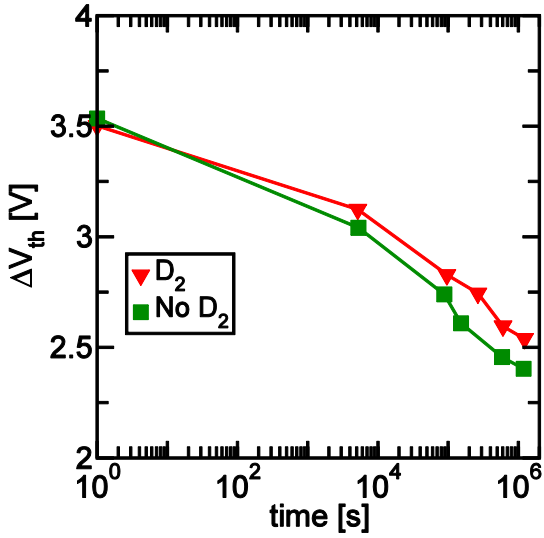


Figure 5.28: Long-term retention measurements for $In_{0.45}Ga_{0.55}As$ channels before and after D_2 annealing. Marginal improvements are observed.

Therefore, different passivation solutions are required to improve the interface and TuOx quality, and to achieve better conduction and memory performance; these solutions could be more invasive than a thermal treatment, as they could require the replacement of the TuOx with other materials. In CMOS technology, it has been demonstrate that ALD Al_2O_3 deposited directly on top of the III-V channel after a Sulfuric pre-treatment is capable to reduce the interface traps [88], [89], and it is preferred over to SiO_2 [89]. Based on these results, an Al_2O_3 layer could be used to replace the TuOx, or could be deposited on top of it to try to improve the interface. However, as the 3-D NAND integration flow is inverted as compared to CMOS technology, the use of an Al_2O_3 layer may give different results and could also have an impact on the memory performance, since the Al_2O_3 would be part of the memory stack.

5.6 Conclusions

Asymmetrical junction study

In order to investigate the impact of the asymmetrical junction (n-type Si source and Ti/TiN drain) of $In_{0.45}Ga_{0.55}As$ devices on the electrical performance, I_D-V_G and I_D-V_D measurements are performed. Different kinds of I_D behavior are observed: I_D-V_D. Independently of where the bias (V_{DS} versus V_{SD}) is applied, I_D can show a rectifying behavior with a drain or a source dominance. Despite the current variability, all I_D-V_G characteristics share a strong saturation.

In order to further understand the current variability, TEM and EDS mapping are conducted and a correlation between the channel morphology/composition and the electrical behavior is found: devices with symmetrical I_D-V_G characteristics have always overgrown channels and are characterized by a constant [*In*] along the memory hole and close to the drain. Devices with rectifying behavior at the source are also characterized by overgrown channels, but show a composition drift with higher [In] close to the drain junction. Finally, devices with rectifying behavior at the drain have always undergrown channels and present material inhomogeneity at the drain side, such as islands of In or Ga, GaAs regions and *Ti-As*.

The intermixing of *Ti-As* is typical in Ti-$In_xGa_{1-x}As$ contacts [160] and leads to bad drain quality. Therefore alternative metals have to be explored to avoid metal/semiconductor mixture.

Simulation-based learning and guideline for devices improvement

TCAD simulations are performed by using Synopsys Sentaurus Device software, with the aim to investigate the impact of channel morphology/composition inhomogeneity on the I_D variability observed in the $In_xGa_{1-x}As$ channels.

Simulations take into account only the electrostatic effects, focusing on electron/hole transport through different materials.

Simulations are able to explain the effect of [*In*] drift close to the Ti drain side: rectifying behavior (with drain dominance) is observed when $In_xGa_{1-x}As$ with low [In], is in contact with Ti. This behavior is caused by the fact that the electron affinity of $In_xGa_{1-x}As$ decreases by reducing the [In], making it smaller than the work function of the *Ti* and leading to the formation of a Schottky contact.

Unfavorable material combination at the drain side (e.g., GaAs in contact with *Ti*, or un-doped III-V in contact with Ti) is detrimental for the

conductivity and increases R_{DS}, leading to a saturation of the I_D-V_G characteristic. On the other hand, Si-doping into the $In_xGa_{1-x}As$ channels, with x higher than 0.45 can cause high levels of I_{off}, as measured in our devices. However, pure electrostatic simulations are not able to explain the rectifying behavior between the III-V and the Si-substrate used as source, as observed in our devices. Ideally III-V in contact with *Si* should lead to an ohmic contact, as also shown by simulations, but in the real devices the situation is different. The lattice mismatch between III-V compounds and Si (e.g., ~4.2% of lattice mismatch for GaAs-*Si* and ~11% between InAs and *Si*) causes interface defects and dislocations [139] (not taken into account in the simulations), which could often lead to the formation of Schottky-contacts instead of ohmic ones [163].

Simulations provide general design guidelines to improve the III-V devices: the I_{off} can be reduced by limiting the channel doping as much as possible. The drain contact can be improved by properly choosing the material and doping level close to the drain: highly doped III-V helps to mitigate the series resistance introduced by the drain, and hence the I_D flattening. Furthermore, InAs is the best candidate as material in contact with the metal drain: high [*In*] helps to lower the Schottky barrier between III-V and *Ti*, leading to an ohmic contact.

Optimization of the drain contact

Simulations have suggested that one of the key parameters to improve the electrical performance of the III-V devices is the use of highly doped III-V close to the drain.

Based on those guidelines, the region in contact with the metal drain is intentionally doped by adding SiH_4 during the III-V growth. An experiment with highly doped III-V close to the source is also conducted to investigate if it is possible to further improve the device performance.

No improvement is observed by deliberately doping the III-V at the source: most probably this region is sufficiently doped by the Si diffusion from the substrate, so that further doping is not required. An improvement of the I_{on} is instead observed when Si-doped InAs is used in contact with the metal drain and the R_D becomes ~5 times lower than the one in the un-optimized devices.

Epi-Si integration and D_2 annealing

Epi-Si is integrated as benchmark material against III-V. As expected, III-V devices show better conduction properties than epi-Si channels, but with a penalty in I_{off} and worse *STS*. The reduced I_{off} values in epi-Si devices are given by the larger Si band gap, which reduces the BTBT mechanism [148], [171], the undoped nature of the epi-Si channel and the better channel/TuOx interface, as indicated by the *STS*.

Epi-Si also shows better retention characteristics than III-V channels, as a consequence of lower density of near-interface TuOx defects. The TuOx quality improvement in epi-Si devices can be related to the higher thermal budget involved during the epi-Si growth and the FGA, that help to cure the TuOx defects as well as the ones at the interface.

D_2 annealing is applied to the III-V channels after the entire wafer processing, to passivate the channel/TuOx interface. Contrary to what reported in literature for 3-D NAND with Si-channels [173] and for III-V nanowires [175], III-V channel/TuOx interface defects cannot be cured by using D_2 annealing passivation; D_2 is not even able to cure the TuOx defects. This indicates that more disruptive passivation solutions are required.

Al_2O_3, traditionally used as gate dielectric in CMOS technology based on III-V channels [88], [89], could be used to replace the SiO_2 as a TuOx, or as an additional thin layer on top of it. However, since CMOS technology always follows a channel-first approach, the use of Al_2O_3 layer may give different results, as already observed with the implementation of D_2 annealing. Al_2O_3 could also have a negative impact on the memory performance, as it will be part of the memory gate stack. In terms of integration, the compatibility between III-V epitaxial growth and a possible new TuOx material has to be verified, to avoid selectivity issues which could cause premature closure of the memory hole during the III-V growth of the channel.

Chapter 6

Conclusions and Outlook

6.1 Conclusions

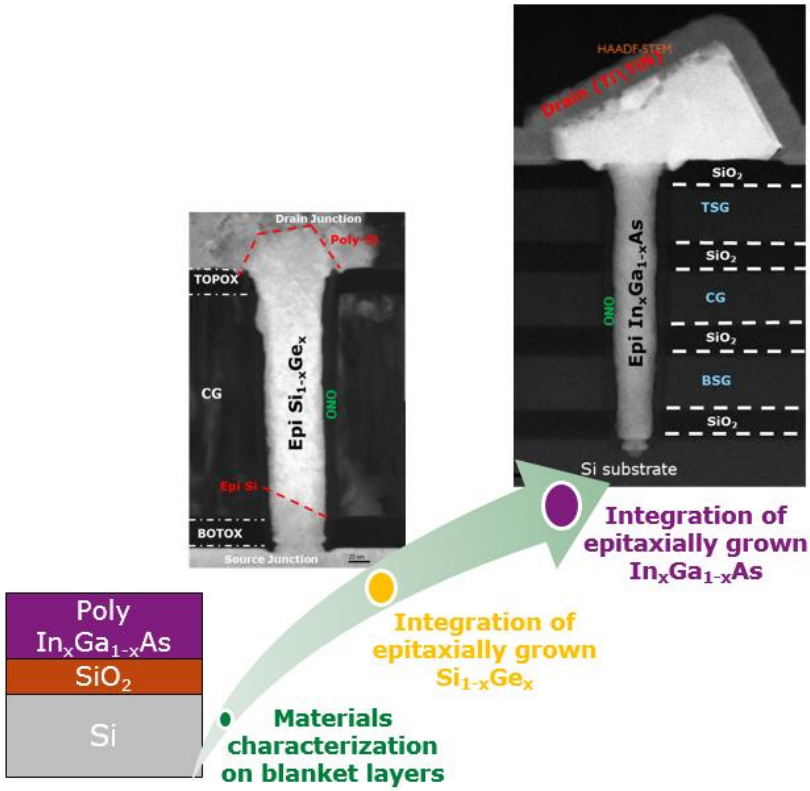


Figure 6.1: Roadmap of the thesis activity.

In this thesis, the feasibility of epitaxially grown III-V channels for future 3-D NAND generations is investigated. Particular attention is given to the most challenging steps of the III-V process integration and to the impact these have on the electrical performance. The research is conducted in three different steps as sketched in Fig. 6.1.

Material characterization on blanket layers

A first screening of InAs, $In_xGa_{1-x}As$ and GaAs is conducted on blanket layers. Two important key parameters are investigated for the selection of the III-V material to be integrated as channel in 3-D NAND memories: mobility and thermal stability.

To perform Hall mobility and Van der Pauw measurements, used for the extraction of mobility and resistivity, the III-V layers are doped with *Si* during the growth. The thermal stability is investigated by applying ex-situ annealing from 300 ˚C up to 500 ˚C in FGA.

The oxidation of GaAs, once such material is exposed to air, results in the formation of stable oxides such as Ga_2O_3 which are difficult to remove, causing a too high contact resistance. The difficulties encountered to contact GaAs, make this material unsuited to replace poly-Si in 3-D NAND channels.

InAs has the best conduction properties. However, there are two factors which could make InAs not suitable as channel material in 3-D NAND: the low band gap (0.36 eV) could prevent the device from switching off and the crystalline structure is not thermally stable, as revealed by the observed grain size increase upon thermal treatments. The thermal stability issues are expected to become more pronounced as the material is transferred from a relaxed geometry (blanket layer) to a constrained geometry such as 3-D NAND memory.

Based on the obtained results, $In_xGa_{1-x}As$ shows a good compromise between electrical characteristics and thermal stability (morphological variations are not observed on this material), the material thus emerging as a promising candidate to replace poly-Si as channel in future 3-D NAND flash memories.

Integration of epitaxially grown $Si_{1-x}Ge_x$

$Si_{1-x}Ge_x$ with a *Ge* concentration of 25 at %, is integrated as channel material in a single cell test vehicle as a stepping stone toward the III-V

channel. Thanks to its better compatibility with the Si-based process flow, $Si_{1-x}Ge_x$ allows us to focus exclusively on the challenges introduced by the poly-Si channel replacement, while keeping other integration steps such as the junction formation unmodified.

The replacement of poly-Si channel with epi-$Si_{1-x}Ge_x$ reveals three main features:

- The surface preparation required to initiate the epitaxial growth appears as a critical step for the memory stack (ONO) integrity. The HCl cleaning used to prepare the surface, conducted in H_2 ambient and it is effective only at high temperature (900 ˚C). At such conditions, the TuOx, which is the memory layer in contact with the channel, is reduced, compromising the memory performance and leading to a significant retention loss.
- The material composition controllability within the memory holes is challenging. A drift of the nominal [*Ge*] from 25 to 40 at % is observed when the $Si_{1-x}Ge_x$ recipe, developed for planar structures, is transferred to our constrained geometries.
- The $Si_{1-x}Ge_x$ growth is not always limited to the memory hole, but can result in overgrowth. The non-uniform growth has an impact on the final channel length, on the position of the drain junction as well as on the drain roughness. The poly-Si drain is locally mixed with the $Si_{1-x}Ge_x$ overgrowth. Therefore, a special drain patterning process has to be developed, to make sure that the drain is properly etched.

Integration of epitaxially grown $In_xGa_{1-x}As$

Based on the initial materials screening conducted on blankets, $In_xGa_{1-x}As$ is integrated as channel material in a three cells test vehicle by MOVPE.

Two alternative cleaning routes, namely using HCl or Cl_2, are investigated for the surface preparation prior to growing the III-V channel; the HCl route uses the same conditions as those implemented in the $Si_{1-x}Ge_x$ integration flow (900 ˚C in H_2).

Contrary to the HCl-based cleaning, Cl_2 is done in N_2 ambient and it dissociates more efficiently at lower temperature (e.g., 600 ˚C), helping to preserve the TuOx thickness, crucial for memory operation. Therefore, the

Cl_2 cleaning represents a promising route to be used for the surface preparation.

The channel composition and filling capability are investigated for several growth conditions. Different channel compositions can be obtained by changing the *In*/*Ga* flow ratio or the deposition temperature: by decreasing the deposition temperature a better incorporation efficiency of In is observed, and channels with higher [*In*] can be achieved.

The III-V channel filling capability is found to be channel diameter and temperature dependent: the percentage of filled devices increases with both the channel diameter and the temperature. However, for high deposition temperature, (e.g., 580 ˚C), selectivity loss is observed: the growth rate increases with temperature, due to a more efficient decomposition of the precursors and the molecules that do not reach the memory holes start to nucleate on the oxide area.

The channel growth rate is variable, as already observed on $Si_{1-x}Ge_x$, leading to different channel lengths. Growth rate variation can be induced by un-balanced material diffusion/transport into the memory holes due to roughness of the memory hole and of the top surface as well as due to the nucleation delay induced by a different starting surface.

The formation of source and drain junctions in Si-reference flow requires a thermal budget as high as 1050 ˚C that is incompatible with $In_xGa_{1-x}As$. To cope with the lower III-V thermal budget, a Ti/TiN stack is used as drain. The patterning of the metal drain is not straightforward. During the metal etch, residues are sputtered on the unexposed metal and on the exposed area (e.g., TSG). Sputtered residues compromise the quality of the final drain contact. Furthermore, they act as a mask, impeding proper etching of the layers underneath (e.g., TSG, CG, BSG), and hence of the gate contacts. To overcome these issues, a tuning of the metal etching process and dedicated cleanings will be required.

The conduction properties of $In_xGa_{1-x}As$ channels, with x ranging between 0.25 and 0.55 are analyzed. Different populations of devices are observed, leading to different values of I_{on} and I_{off}. By conducting TEM and EDS mapping of the typology of the studied devices, a correlation between the electrical performance and the channel composition is found: devices with low current (e.g., $I_{on} < 1$ nA) are characterized by a variable [*In*] in the channel and by the presence of *In* clusters. If the *In* clusters are in the center of the channel, the current appears as un-modulated. Devices with high current and good modulation (e.g., $I_{on}/I_{off} > 100$) show instead almost constant [*In*] along the channel.

As observed on blankets, the $In_xGa_{1-x}As$ conduction properties improve by increasing the [*In*], but at the expense of the I_{off}. Indeed, as the [*In*] increases the band gap of the $In_xGa_{1-x}As$ is reduced, enhancing BTBT mechanisms. However, there are also other factors responsible for the increase in I_{off} such as traps at the interface between the channel and the TuOx and possible diffusion of *Si* from the substrate during the III-V growth, that acts as n-type dopant.

The I_D-V_G characteristics are characterized by a rectifying behaviors either at the drain or at the source side and they always show a flattening starting above 1 V of V_G. TEM and EDS show that devices with rectifying behavior at the drain are characterized by undergrown channels with material inhomogeneity at the drain side (e.g., *In* and *Ga* clusters, Ti-As and GaAs regions), as a consequence of Ti-$In_xGa_{1-x}As$ intermixing. Devices showing rectifying behavior at the source suffer from overgrown channels with a higher [*In*] close to the drain.

Pure electrostatic simulations are carried out to investigate the impact of channel composition/morphology inhomogeneity on the I_D variability. These are able to explain the effect of [*In*] drift at the drain side: rectifying behavior at the drain is observed when GaAs is in contact with *Ti*. This behavior is caused by the fact that the electron affinity of GaAs is smaller than the work function of the *Ti*, leading to the formation of a Schottky contact. The unfavorable material combination at the drain side (e.g., GaAs in contact with *Ti*, or un-doped III-V in contact with *Ti*) is detrimental for the conductivity and increases the drain series resistance, leading to a flattening of the I_D-V_G characteristic. Simulations are not able to explain the rectifying behavior between the III-V and the Si-substrate, used as source. The Schottky contact at the source side might be caused by misfit and threading dislocations (not simulated) caused by the large lattice mismatch between the III-V and Si (e.g., ~ 4.2% of lattice mismatch for GaAs-*Si* and ~11% between InAs and *Si*).

Simulations give a guideline to improve the device: a significant reduction of the I_{off} can be achieved by reducing as much as possible the doping into the channel. On the other hand, highly doped III-V close to the metal drain helps to mitigate the series resistance introduced by the drain, and hence the I_D flattening. Furthermore, InAs is the best candidate material in contact with the metal drain: high [*In*] helps to lower the Schottky barrier between the III-V and the *Ti*, leading to an ohmic contact.

Based on the pathway suggested by the simulations, devices with optimized drain are integrated: highly *Si* doped InAs is used at the drain side

instead of undoped $In_{0.45}Ga_{0.55}As$. The drain optimization results in ~ 5 times lower drain resistance than the one of unoptimized devices.

$In_{0.45}Ga_{0.55}As$ channels show superior conduction properties compared to the poly-Si reference: Scalpel SPM technique reveals that the III-V channels conductivity is increased by a factor of 1000 with respect to the one in poly-Si. The conduction properties of epitaxially grown III-Vs are also improved with respect to the ones in epi-Si channels, but at a penalty in I_{off} and *STS*. As already mentioned, the higher I_{off} observed in III-Vs can be caused by their lower band gap, the presence of n-type impurities in the channel and defects at the channel/SiO_2 interface, as indicated by the *STS*. Defects at the interface can play a role because of the absence of a passivation step as well as by possible incompatibility between III-V and SiO_2.

D_2 annealing is applied to the III-V channels after the entire wafer processing, to passivate the channel/TuOx interface. Contrary to what is reported in literature for *Si* channels, these defects cannot be cured by D_2 annealing.

P/E measurements can be performed on the III-V devices, but the retention is compromised by a defective TuOx. The defects in the TuOx can be partially cured by low temperature thermal treatments, or by replacing the HTO procedure by PEALD of TuOx.

6.1 Future Work

This work has focused on the most challenging steps to integrate higher electron mobility materials in full channels 3-D NAND. However, in expanding this work, several additional improvements and investigations could be done.

It is important to develop a stable process to limit as much as possible the channel variability (e.g., composition drift, segregation of [*In*]) that affects the electrical performance.

An in-depth investigation of the metal drain is required to avoid the metal/III-V channel intermixing which hampers the device performance.

Passivation techniques have to be explored to reduce the near-interface TuOx defects that limit the memory performance.

The learning generated on full channel can be transferred to a more industrially relevant structure such as the Macaroni channel. The latter probably requires the use of ALD as deposition technique, to guarantee a conformal deposition of the thin channel on top of the ONO memory stack.

The use of ALD could have advantages and disadvantages with respect to the MOCVD approach used in this thesis: the channel will be polycrystalline, with a penalty in the conduction properties. On the other hand, it opens more options for the exploration of layers to improve the interface between the III-V channel and the memory gate stack. Moreover, it might also overcome the possible Si-diffusion from the substrate into the channel, as the deposition temperatures for ALD are lower, leading to a reduction of the I_{off}. A further reduction of the I_{off} level is expected in the Macaroni approach, as result of the thin channel that can be better controlled by the control gate.

Curriculum Vitae

Elena Capogreco was born in Locri, Italy, on March 8, 1988. She received the Bachelor degree in electronic engineering in 2010 and her M.Sc. degree in electronic engineering in 2012 at Universita'della Calabria (UniCal), Italy. During her M.S. degree she spent six months of study at Universidad Autonoma de Barcelona (UAB), Spain, trough Erasmus Student Exchange. Then, she joined seven months the Interuniversity Micro-Electronics Center (imec), Belgium, for her M.S. thesis with Erasmus Placement Exchange. Her M.S. thesis dealt with Leakage Mechanism in Ultra-Thin high-k MOSFETs'. In April 2013, she started her doctoral studies in Flash Memory Devices at imec and at KU Leuven on the topic "Alternative channel materials for 3-D NAND memories". Since April 2017, she is working at imec as process integration engineer.

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